SERVICE MANUAL FOR

8555

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Oct.2003

MiTAC

8555 N/B Maintenance

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1. Hardware Engineering Specification

1.1 Introduction

This document describes the system hardware engineer specification for 8555 portable notebook computer system. The 8555 notebook computer is a new mainstream high performance thin and light notebook in the MiTAC notebook family.

1.2 System Overview

CPU	- Intel DT Pre-Scott 3.2G, 3.4G, 3.6G backward compatible with DT Northwood P4 2.4G, 2.6G, 2.8G, 3.06G, 3.2G, 3.4GHZ or above w/z HT, FSB 800/533 & Celeron FSB400
Core Logic	- **SiS648FX (Co-Layout with SiSM661(P)) + SiS963**
L2 Cache	- 512KB OD for P4, 128KB for Celeron, 1M for Pre-Scott
System BIOS	- Insyde 256 KB(P) Flash EPROM (Include System BIOS and VGA BIOS) - ACPI 1.0b; DMI 2.3.1 compliant - Plug & Play capability
Memory	- 0MB on board; Expandable up to 1024MB - Expandable with combination of optional 128/256/512 MB memory - 200-pin DDR 333/400 DRAM Memory Module x2
ROM Drive	- 12.7mm Height - 24X CD ROM Drive - 8X DVD ROM Drive - 8X8x24 CD-RW or above - 24X10X8X24 Combo or above - Super Combo DVD-RW
HDD	- 2.5" 9.5 mm height: 20/30/40/60 GB; Support Ultra DMA 66/100 - Changeable for Distributor
FDD	- Support External FDD w/z USB I/F; 3.5 Format for 720KB/1.2MB/1.44MB

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Display	- 14.1" XGA TFT Display; Resolution: 1024x768 - 15" XGA/ SXGA+ TFT Display; Resolution: 1024X768 /1400x1050
Video Controller	- ATI M9+X with **external** 64MB VRAM**/ M10P (reserved)**
Keyboard	- 19mm key pitch/ 3.0mm key stroke/ 307mm length - Windows Logo Key x 1; Application Key x 1
Pointing Device	- Glide pad with 2x buttons and 4 direction scroll button
PCMCIA	- TypeII X1 Without ZV -Cardbus Support
4 in 1 Card reader	- Card Reader SD/SM/MMC/MS
Indictor	- 3 LEDs for Power/Battery/Charge status (on display housing) - 1 LED for Radio wave status Power LED (blue) (BTO: Wireless LAN only) - 5 LEDs for HDD Access, ODD Access , Num lock, Cap lock and Scroll Lock - 1 LED for Card reader status
Audio System	- Sound Blaster Pro compatible - AC97 V2.1 Codec - Built-in Mono Microphone - 2X Speaker (w/z sound chamber)
I/O Port	- USB port (2.0, backward compatible with USB1.1) x 4 - Bidirectional Parallel port (EPP/ECP) x 1 - RJ-11 port x 1 - RJ-45 port x 1 - DC input x 1 - VGA monitor port x1 - Audio-out x 1 (S/P DIF) - Mic-in x 1 - Hardware Volume Control - S Video TV-Out x 1 (NTSC/PAL) - IEEE1394a x 1 - Mini PCI
Communication	- Built-in 56Kbps V.90 modem - Built-in 10/100 M based-T LAN - One Mini PCI slot and one antenna reserved for wireless LAN
AC adapter	- Universal AC adapter 150W ; Input: 100-240V, 50/60Hz AC (support power on charge)
Battery	- 12 cell (2200mAH/3.7V) Li-ion standard
Dimensions	- 332x285x39.7(max)
Weight	- 3.5kg (P)
Accessories	- Power Cord, AC Adapter, RJ-11 Phone Cable, Manual, System Driver CD-Title
Manual Printings	- EN, GR, CH, Pan-EU
Agency	- FCC, CE, UL, TUV, CB, BSMI
Architecture	- Support PC2001 Specification, Designed for Windows XP(driver ready for 98,ME, and 2000)
Options	- 128/256/512MB DDR SDRAM, AC Adapter w/o Power Cord, Notebook Carry Bag

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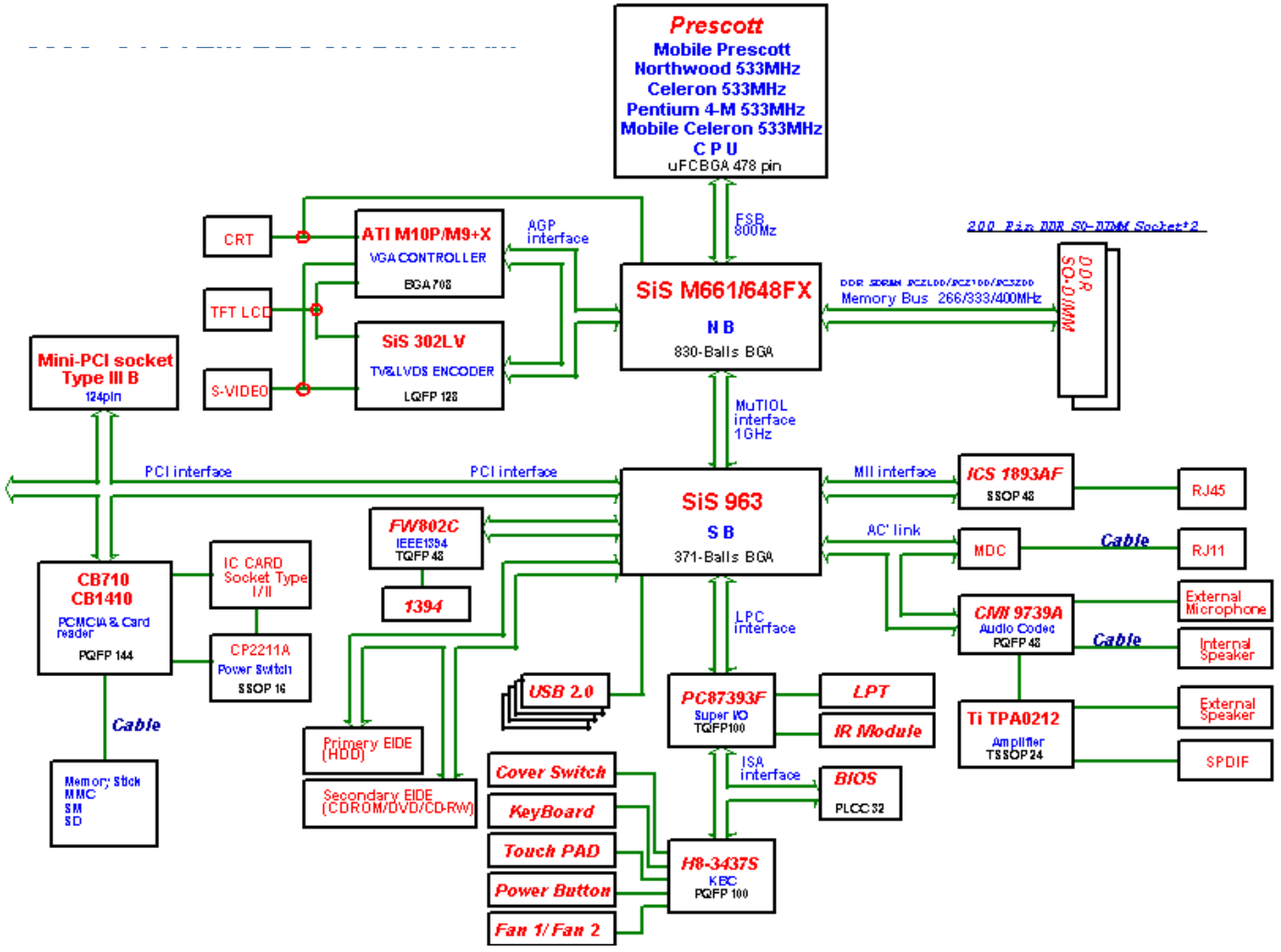
1.3 System Architecture

1.3.1 Block Diagram



1.3.2 Function Description

1.3.2.1 CPU

- Socketable Intel D/T&Mobile Pentium 4 Prescott / Northwood / Celeron processors with 400/533/800MHz FSB.
- Capable of mFC-PGA processor package.
- Support 8KB L1 Cache and 256/512/1000 KB L2 Cache (Depends On CPU)

1.3.2.2 CORE LOGIC

- SiS 648FX Memory Control Hub.
  - Dynamic Clock Enable (CKE) control
  - Support AGP 3.0 Compliant
  - High Throughput SiS MuTIOL connects to SiS963 MuTIOL Media I/O
  - 830-Balls BGA Package.
- SiS 963 Internal Connect Hub.
  - Integrates one Universal Serial Bus 2.0 Host Controllers.
  - Integrates the 1394a Controller
  - Integrates the Audio Controller with AC97 Interface.
  - Integrates the Ethernet MAC Controller W/ standard MII interface.

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- Integrates three Universal Serial Bus 1.1 Host Controllers.
- Integrates the IDE Master/Slave controllers
- Supports SiS MuTIOL technology.
- Integartes the PCI to LPC bridge
- Integrates I/O Advanced Programmable Interrupt Controller
- Integrates legacy system I/O and legacy power management functionalities.

1.3.2.3 MEMORY

- Support unbuffer DDR 200/266/333/400MHz SO-DIMM expandable to 1024MB (2 DDR-SODIMM slots).

Slot1	Slot2	Total
64MB	0	64MB
64MB	64MB	128MB
64MB	128MB	192MB
64MB	256MB	320MB
64MB	512MB	576MB
128MB	0	128MB
128MB	128MB	256MB
128MB	256MB	384MB
128MB	512MB	640MB
256MB	0	256MB
256MB	256MB	512MB
256MB	512MB	768MB
512MB	0	512MB
512MB	512MB	1024MB

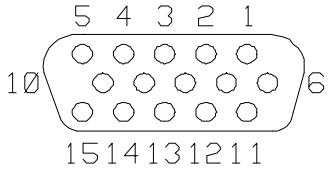
1.3.2.4 I/O PORTS

- **CRT Port**

  - Standard VGA compatible port

  - C1 and DDC2B compliant

PIN	SIGNAL	DESCRIPTION
1	RED	Red analog video output
2	GREEN	Green analog video output
3	BLUE	Blue analog video output
4	Monitor Sense	NC
5	GND	Monitor Sense
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	VCC	+5VDC
10	GND	Ground
11	Monitor Sense	NC
12	CRT DATA	Data from DDC monitor
13	HSYNC	Horizontal Sync control
14	VSYNC	Vertical Sync control
15	CRT CLK	Clock to DDC monitor



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CRT Sport Mode

Resolution	DCLK	Page Size	Band Width	DRAM Size
1024x768x8@60NI	65Mhz	0.768MB	65MB/s	1MB
1024x768x16@60NI	65Mhz	1.536MB	130MB/s	2MB
1024x768x32@60NI	65Mhz	3.072MB	260MB/s	4MB
1024x768x8@75NI	78.75Mhz	0.768MB	78.75MB/s	1MB
1024x768x16@75NI	78.75Mhz	1.536MB	157.5MB/s	2MB
1024x768x32@75NI	78.75Mhz	3.072MB	315MB/s	4MB
1024x768x8@85NI	94.5Mhz	0.768MB	94.5MB/s	1MB
1024x768x16@85NI	94.5Mhz	1.536MB	189MB/s	2MB
1024x768x32@85NI	94.5Mhz	3.072MB	398MB/s	4MB
1280x1024x8@60NI	108Mhz	1.28MB	108MB/s	2MB
1280x1024x16@60NI	108Mhz	2.56MB	216MB/s	4MB
1280x1024x32@60NI	108Mhz	5.12MB	432MB/s	6MB
1280x1024x8@75NI	135Mhz	1.28MB	135MB/s	2MB
1280x1024x16@75NI	135Mhz	2.56MB	270MB/s	4MB
1280x1024x32@75NI	135Mhz	5.12MB	540MB/s	6MB
1280x1024x8@85NI	157.5Mhz	1.28MB	157.5MB/s	2MB
1280x1024x16@85NI	157.5Mhz	2.56MB	315MB/s	4MB
1280x1024x32@85NI	157.5Mhz	5.12MB	630MB/s	6MB
1600x1200x8@60NI	162Mhz	1.875MB	162MB/s	4MB
1600x1200x16@60NI	162Mhz	3.75MB	324MB/s	4MB
1600x1200x32@60NI	162Mhz	7.5MB	648MB/s	8MB
1600x1200x8@75NI	202.5Mhz	1.875MB	202.5MB/s	4MB
1600x1200x16@75NI	202.5Mhz	3.75MB	405MB/s	4MB
1600x1200x32@75NI	202.5Mhz	7.5MB	910MB/s	8MB
1600x1200x8@85NI	230Mhz	1.875MB	230MB/s	4MB
1600x1200x16@85NI	230Mhz	3.75MB	460MB/s	4MB
1600x1200x32@85NI	230Mhz	7.5MB	920MB/s	8MB
1920x1440x8@85NI	330Mhz	1.875MB	230MB/s	4MB
1920x1440x16@85NI	330Mhz	3.75MB	460MB/s	4MB
1920x1440x32@85NI	330Mhz	7.5MB	920MB/s	8MB
2048x1536x8@75NI	333Mhz	3MB	255MB/s	8MB
2048x1536x16@75NI	333Mhz	6MB	510MB/s	8MB
2048x1536x32@75NI	333Mhz	12MB	1.2GB/s	16MB
2048x1536x8@75NI	333Mhz	3MB	255MB/s	8MB
2048x1536x16@75NI	333Mhz	6MB	510MB/s	8MB
2048x1536x32@75NI	333Mhz	12MB	1.2GB/s	16MB

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- **7 Pins S-VIDEO port for TV-Out**

  - Support up 1024*768 resolution

  - Support PAL and NTSC system

  - Support Composite Output by a transfer cable.

S-Video Port

PIN	SIGNAL NAME	DIRECTION
1	GND	-
2	NC	-
3	COMP	O
4	GND	-
5	CRMA	O
6	NC	-
7	LUMA	O

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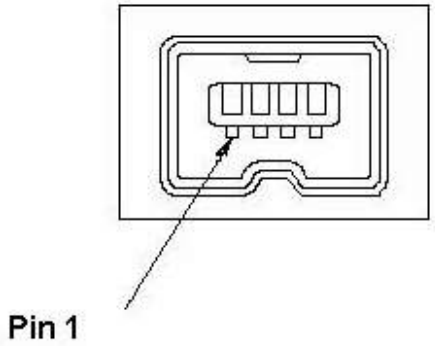
TV Out Support Modes

System	Input(Active) Resolution	Active TV lines	Over/Under scan
NTSC	320x200	480 ~ 400	+
NTSC	640x480	480 ~ 400	+
NTSC	720x480	480 ~ 400	+
NTSC	720x400	480 ~ 400	+
NTSC	800x600	480 ~ 420	+
NTSC	1024x768	480	Over
System	**Input(Active) Resolution**	**Active TV lines**	**Over/Under scan**
PAL	320x200	540 ~ 500	+
PAL	640x480	540 ~ 500	+
PAL	720x400	540 ~ 500	+
PAL	720x576	576 ~ 510	+
PAL	800x600	600 ~ 510	+
PAL	1024x768	520	Under

- **IEEE1394A Port**

PIN	SIGNAL NAME	DIRECTION
1	TPB-	I/O
2	TPB+	I/O
3	TPA-	I/O
4	TPA+	I/O



- **Audio Ports**

  - SPDIF

  - Microphone In

  - Built In 2 high quality internal speaker (2W/4ohm w/ Box)

  - Built in 1 mono microphone

  - AC97 V2.2 compliance.

	Internal Speaker	Internal Microphone	LED Of SPDIF
Plug Ear-Phone In	Mute	Active	Off
Plug SPDIF Device In	Mute	Active	On
Plug External Microphone	Active	Mute	Off

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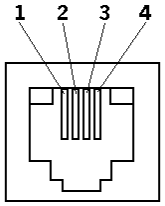
- **RJ-11**

  - Connection to Modem Daughter Board Connector or Mini-PCI Modem Card.

  - Support 56Kbps/V.92 .

Pin	Signal Name	Direction	Description
1	NC	-	No Connect
2	LINE +	I/O	Phone Line Positive
3	LINE -	I/O	Phone Line Negative
4	NC	-	No Connect



- **RJ-45**

  -The Fast Ethernet MAC Controller features an IEEE802.3 and IEEE802.3x compliant MAC with externalLAN physical layer chip (ICS1893AF) supporting full duplex 10 Base-T,100 Base-T Ethernet.

  -Support Wake-On-LAN function in System enter to S1,S3.

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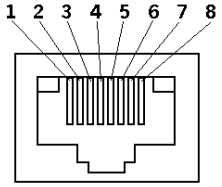
Pin	Signal Name	Direction	Description
1	TX+	Out	Transmit Data Ring
2	TX-	Out	Transmit Data Tip
3	RX+	IN	Receive Data Ring
4	TERM 1	-	Internal termination resistor
5	TERM 2	-	Internal termination resistor
6	RX	IN	Receive Data Tip.
7	TERM 3	-	Internal termination resistor
8	TERM 4	-	Internal termination resistor



- **Infrared interface supporting IrDA format**

  - FIR IrDA 1.1 compliant.

  - Sharp -SIR supported.

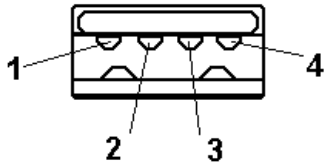
  - Support distance 1M

- **USB Ports**

  - Four industry standard USB 2.0 ports (Backward compatible to USB 1.1)

  - Support maximum transfer rate up to 480Mbits/s

Pin	Signal Name	Direction	Description
1	VCC	Power	USB Device Power (+5VDC)
2	DATA-	I/O	Balanced Data Negative
3	DATA+	I/O	Balanced Data Positive
4	GND	Power	Ground



- **PS/2 Ports**

  - Support Mouse and Keyboard via a Y-Type cable.

- **Parallel Ports**

  - Configurable as logical ports LPT1 , LPT2 or LPT3

  - EPP rev 1.7 & 1.9 compatible

  - ECP (IEEE 1284) compatible

  - Industry standard 25 Pins connector

  - IEEE1284 Compliant.

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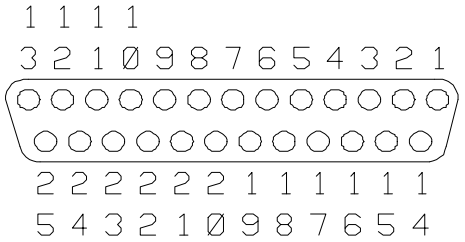
Pin	Signal Name	Direction	Description
1	STROBE#	O	Data Strobe
2	PD0	I/O	PP Data bit 0
3	PD1	I/O	PP Data bit 1
4	PD2	I/O	PP Data bit 2
5	PD3	I/O	PP Data bit 3
6	PD4	I/O	PP Data bit 4
7	PD5	I/O	PP Data bit 5
8	PD6	I/O	PP Data bit 6
9	PD7	I/O	PP Data bit 7
10	ACK#	I	Printer Acknowledge
11	BUSY	I	Printer Busy
12	PE	I	Paper Out
13	SLCT	I	Print Select Acknowledge
14	AUTOFDXT#	O	Auto Line Feed
15	ERROR#	I	Printer Error
16	INIT#	O	Reset Printer
17	SLCTIN#	I	Select In
18	GND	-	Ground
19	GND	-	Ground
20	GND	-	Ground
21	GND	-	Ground
22	GND	-	Ground
23	GND	-	Ground
24	GND		Ground
25	GND	-	Ground
Case	GND	-	Ground



1.3.2.5 PC CARD SLOT

- One Type II/I slot supporting the 1997 PC Card standard,and including full R2 (16-bit) and 32-bit Cardbus data transfer
- ENE CB710 (PCMCIA Controller) & ENE CP2211 (Power Switch)
- Ability to wake-up from D3-Hot and D3-Cold.
- Mixed-and-match 5V/3.3V 16 bits PC CARDs and 3.3V Cardbus Card.

1.3.2.6 GRAPHICAL SUBSYSTEM

- ATI M9+X & M10-P graphical controller embedded 64MB DDR VRAM
- AGP 8X Interface.

1.3.2.7 DISPLAY

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- Internal LCD Display is 15.1”/14.1” TFT ISP XGA/SXGA+ color
- Dual View of LCD+CRT / LCD+TV independent display.
- External Video refresh rate of up to 100Hz supported
  - Vertical refresh frequencies to meet VESA requirements
  - Simultaneous video in specified video modes – switchable with hot key

1.3.2.8 IDE INTERFACE

- Support Dual Independent IDE Channels, One is Hard-Disk. The other one is Optical Device.
- Supports PIO mode 0,1,2,3,4 and Ultra DMA 33/66/100.

1.3.2.9 READ ONLY MEMORY (BIOS FLASH)

- Fully compatible with industry standard software including Windows 2000 & Windows XP
- Fully supports APM V1.2 and latest ACPI specification
- 2Mb Flash BIOS
- Insyde BIOS core

1.3.2.10 POWER MANAGEMENT FEATURES

- Local standby mode (Individual devices such as HDD, graphics controller, LCD etc..)
- CPU Idle mode (Including ACPI modes C1 and C2)
- Suspend mode (Including S1 and S3 ACPI modes)
- Fully APM V1.2 compliant
- Fully ACPI V1.1 compliant
- Hibernate for Windows 2000 and Windows XP
- Thermal management
- Fully US EPA Energy Start compliant

1.3.2.11 KEYBOARD CONTROLLER

- Hitachi H8-3437S

1.3.2.12 SUPER I/O

- NS PC87393F LPC interface Ultra I/O

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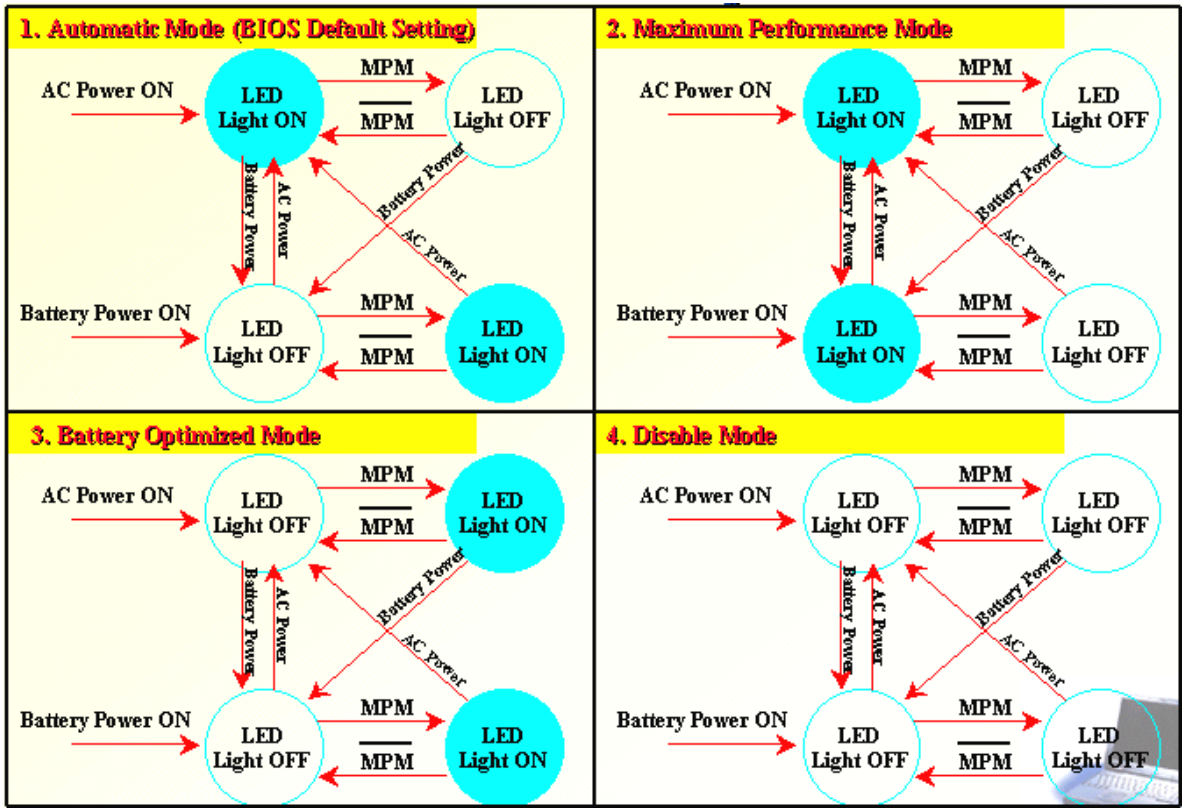
1.3.2.13 LEDs INDIACTOR

- CDROM & HDD & NUM & CAP & SCROLL & Wireless Indicator

1.3.2.14 BUTTONs

- One MPM Button w/z Blue LED



1.3.2.15 TOUCH PAD MODULE

- Synaptics TM41PU-311 with two Buttons

1.3.2.16 MODEM (MDC) - Option

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	MONO_OUT	2	NC
3	GND	4	MODEM_SPK
5	NC	6	NC
7	NC	8	GND
9	NC	10	+5V
11	NC	12	NC
13	NC	14	NC
15	GND	16	Pull Up to +3V
17	+3V	18	+5V
19	GND	20	GND
21	+3V	22	ACSYNC
23	ACSDOUT	24	MSDIN
25	-ACRST	26	MSDIN
27	GND	28	GND
29	GND	30	ACBITCLK

1.3.2.17 Card Reader(8555)

- Support Smart-Media, SD , Memory Stick , MultiMediaCard
- Support Cardreader type.

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Type	Memory Stick	SmartMedia	MultiMediaCard	SD memory card
Picture				
Size(mm)	21.5x50x2.8	37x45x0.76	24x32x1.4	24x32x2.1
Weight (g)	4	2	1.5	2
Volume(mm^3)	3,010	1,265	1,075	1,612
Developer	Sony Corp.('98)	TOSHIBA Corp.('95)	Siemens AG. SanDisk Corp. ('97)	Matsushita Electronic Industrial CO., Ltd. TOSHIBA Corp. SanDisk Corp. ('00)
No. of pins	10	22	7	9
Storage capacity (MB)	8, 16, 32, 64 and 128 (due for release in '01)	4 - 64	4 - 64	8 - 64
Data transfer rate	1.8MB/s Max.(W) 2.45MB/s Max.(R)	-	-	-
Copyright protection	Adherence to SDMI (MagicGate)	ID	ID	Adherence to SDMI

1.4 Electrical Characteristic

1.4.1 SiS963 GPI/O Pin Define

Pin Name	Mux Function	GPIO Function	Power Plane	Signal Name	Type
GPIO0	SPDIF	GPIO	MAIN	ENABKL_MSK#	
GPIO1	LDRQ1#	GPIO	MAIN	MPCIACT#	Input
GPIO2	THERM#	GPIO	MAIN	SB_THRM#	
GPIO3	EXTSMI#	GPIO	MAIN	EXTSMI#	
GPIO4	CLKRUN#	GPIO	MAIN	CLKRUN#	
GPIO5	PREQ5#	GPIO	MAIN	MPCI_PD	Input
GPIO6	PGNT5#	GPIO	MAIN	SPK_OFF#	Output
GPIO7	GPWAK#	GPIO	AUX		
GPIO8	RING	GPIO	AUX	WAKE_UP#	
GPIO9	AC_SDIN2	GPIO	AUX	SCI#	
GPIO10	AC_SDIN3	GPIO	AUX	CRT_IN#	
GPIO11	STP_PCI# / CLK25M	GPIO	AUX	STP_PCI#	
GPIO12	CPUSTP#	GPIO	AUX	CPU_STP# / DPSLP#	
GPIO13	DPRSLPVR	GPIO	AUX	DPRSLPVR	
GPIO14	AGPSTOP#/S3AUXSW#	GPIO	AUX	AGP_STOP#	
GPIO15	KBDAT / VR_HILO#	GPIO	AUX		
GPIO16	KBCLK / LOHI#	GPO	AUX	CPUPERF#	
GPIO17	PMDAT / VGATEM	GPO	AUX	NUM#	
GPIO18	PMCLK / RTC32KHZ	GPO	AUX	CAP#	
GPIO19	Reserved for CLK	GPIO	AUX	SMBCLK	
GPIO20	Reserved for Data	GPIO	AUX	SMBDATA	
GPIO21	EESK	GPI	AUX	EESK	
GPIO22	EEDI	GPI	AUX	EEDI	
GPIO23	EEDO	GPI	AUX	EEDO	
GPIO24	EECS	GPI	AUX	EECS	
APICD0	THERM2#		MAIN(GTL LEVEL)		
APICD1	GPIOFF#		MAIN(GTL LEVEL)		
APICCLK	LDTREQ# / AGPBUSY#		MAIN		
OC5	GPI	GPI	AUX		

	MINI-PCI	CB710	CARD BUS
PCI Interrupt	INTD#	INTB# / INTC#	INTB#
PCI Bus Request	REQ2#	REQ0#	REQ0#
PCI Bus Grant	GNT2#	GNT0#	GNT0#
ID Select	AD21	AD20	AD20

1.4.2 Keyboard Controller Pin Define

Pin	Port	Signal Name	Type	Description
79~72	P10~P17	KO[0..7]	O	Keyboard Matrix
67~60	P20~P27	KO[8..15]	O	Keyboard Matrix
82~89	P30~P37	SD[0..7]	I/O	ISA Data Bus
49	P40	MAINPWR	O	Control S3 off power
50	P41	H8_WAKE_UP#	O	Connect to chipset SiS962 to wake up system
51	P42	H8_SMI#	O	Connect to chipset SiS962 to system management interrupt(Non-ACPI mode)
52	P43	H8_SCI	O	Connect to chipset SiS962 to system configuration interrupt(ACPI mode)
53	P44	IRQ1	O	IRQ For Keyboard
54	P45	IRQ12	O	IRQ For Mouse
55	P46	FAN0#	O	Control CPU Core D/D FAN (Second FAN) ON & Turn ON/OFF Duty
56	P47	FAN1#	O	Control CPU FAN ON & Turn ON/OFF Duty
14	P50	PWR_ON	O	Control System Power ON/OFF
13	P51	NC	NC	X
12	P52	LEARNING#	O	Control Charger Circuitry for Battery Learning
26~29	P60~P67	KI[0..7]	I	Keyboard Matrix
1	RESET	H8_RESET#	I	Reset H8-3437S
7	NMI#	H8_SUSB	I	STR Indicator,High:STR,Low:Normal Operation.
8	STBY	H8_STBY#	I	RC
10	PA7	T_CLK	I/O	Connect to Touch Pad clock
11	PA6	NC	NC	X
20	PA5	NC	NC	X
21	PA4	PSON#_H8	O	System Power Ready.
30	PA3	ADEN#	I	ADAPTOR IN

Pin	Port	Signal Name	Type	Description
31	PA2	NC	NC	X
47	PA1	BATT_DEAD#	I	Indicated the battery capacity is not enough to power on system
48	PA0	RI#	I	If system on suspend mode, then received this signal & system have to wake up
57	PB7	T_DATA	I/O	Connect to touch Pad DATA
58	PB6	SCROLL#	OD	SCROLL# LED
68	PB5	NC	NC	X
69	PB5	NC	NC	X
80	PB3	FAN1_SPD	I	Return FAN1 (CPU FAN) Speed.
31	PA2	NC	NC	X
47	PA1	BATT_DEAD#	I	Indicated the battery capacity is not enough to power on system
48	PA0	RI#	I	If system on suspend mode, then received this signal & system have to wake up
57	PB7	T_DATA	I/O	Connect to touch Pad DATA
58	PB6	SCROLL#	OD	SCROLL# LED
68	PB5	NC	NC	X
69	PB5	NC	NC	X
80	PB3	FAN1_SPD	I	Return FAN1 (CPU FAN) Speed.
81	PB2	FAN0_SPD	I	Return FAN0 (CPU Core D/D FAN) Speed.
90	PB1	BATT_POWER#	O	BATTERY LED
91	PB0	AC_POWER#	O	AC LED
5	MD1	H8_MODE1	I	H8 Mode select
6	MD0	H8_MODE0	I	H8 Mode select
16	P97	BAT_DATA	I/O	SM_BUS DATA For Smart Battery.
17	P96	BATT_G#	O	Battary green LED

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Pin	Port	Signal Name	Type	Description
18	P95	H8_SISPWRBTN#	O	Button to SiS962
19	P94	SW_+5VA	O	To switch +5V/+5VA power source
22	P93	H8_THRM#	O	TO SiS962,REGUSTANG THE SYSTEM TOENTER POWER MANGMENT MODE,Clock Throttling.
23	P92	POWERBTN#	I	System power button
24	P91	LID#	I	Cover switch,Logic Low means LCD Cover Closed.
25	P90	H8_SUSC	I	System inter S4~S5,High:STD or Power Off,Low:Normal Operation.
99	P86	BAT_CLK	I/O	SM_BUS Clock For Smart Battery.
98	P85	H8_MCCS#	I	Port 60h/64h Chip Select.
97	P84	IOW#	I	INPUT/OUTPUT WRITE
96	P83	IOR#	I	INPUT/OUTPUT READ
95	P82	H8_KBCS#	I	Port 62h/66h Chip Select.
94	P81	BATT_R#	O	Battary red LED
93	P80	SA2	I	ISA ADDRESS
45	P77	BLADJ	O	Back / Light Adjust Control
44	P76	CHG_I	O	
43	P75	POWER THRM	I	Monitor Thermal of D/D for CPU Core.
42	P74	I_DISCHG	I	Current sensor
41	P73	I_CHG	I	Current sensor
40	P72	I_LIMIT	I	FOR BATTERY CHARGE
39	P71	BAT_VOLT	I	Report Battery Voltage
38	P70	BAT_TEMP	I	Report Battery Thermal

1.4.3 Power Consumption Of Suspend Mode

- Suspend To RAM < 100mA
- Suspend To Disk / Soft-Off /Mechanical Off < 1mA

1.4.4 Clock Harmonic List

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	12M	12.288M	14.318M	16M	24M	24.576M	25M	27M	32.768K	33M	48M	65M	66M	100M
1	12MHz	12.288MH	14.318MHz	16MHz	24MHz	24.576MHz	25MHz	27M	32.768KHz	33MHz	48MHz	65MHz	66MHz	100MHz
2	24MHz	24.576MH	28.636MHz	32MHz	48MHz	49.152MHz	50MHz	54M	65.536KHz	66MHz	96MHz	130MHz	132MHz	200MHz
3	36MHz	36.864MH	42.954MHz	48MHz	72MHz	73.728MHz	75MHz	81M	98.304KHz	99MHz	144MHz	195MHz	198MHz	300MHz
4	48MHz	49.152MH	57.272MHz	64MHz	96MHz	98.304MHz	100MHz	108M	131.072KHz	132MHz	192MHz	260MHz	264MHz	400MHz
5	60MHz	61.44MHz	71.59MHz	80MHz	120MHz	122.88MHz	125MHz	135M	163.84KHz	165MHz	240MHz	325MHz	330Mhz	500MHz
6	72MHz	73.728MH	85.908MHz	96MHz	144MHz	147.456MHz	150MHz	162M	196.608KHz	198MHz	288MHz	390MHz	396Mhz	600MHz
7	84MHz	86.016MH	100.226MHz	112MHz	168MHz	172.032MHz	175MHz	189M	229.376KHz	231MHz	336MHz	455MHz	462Mhz	700MHz
8	96MHz	98.304MH	114.544MHz	128MHz	192MHz	196.608MHz	200MHz	216M	262.144KHz	264MHz	384MHz	520MHz	528Mhz	800Mhz
9	108MHz	110.592MI	128.862MHz	144MHz	216MHz	221.184MHz	225MHz	243M	294.912KHz	297MHz	432MHz	585MHz	594MHz	900Mhz
10	120MHz	122.88MH	143.18MHz	160MHz	240MHz	245.76MHz	250MHz	270M	327.68KHz	330MHz	480MHz	650MHz	660MHz	1GHz
11	132MHz	135.168MI	157.498MHZ	176MHz	264MHz	270.336MHz	275MHz	297M	360.448KHz	363MHz	528MHz	715MHz	726MHz	1.100GHz
12	144MHz	147.456MI	171.816MHz	192MHz	288MHz	294.912MHz	300MHz	324M	393.216KHz	396MHz	576MHz	780MHz	792MHz	1.200GHz
13	156MHz	159.744MI	186.134MHz	208MHz	312MHz	319.488MHz	325MHz	351M	425.984KHz	429MHz	624MHz	845MHz	858MHz	1.300GHz
14	168MHz	172.032MI	200.452MHz	224MHz	336MHz	344.064MHz	350MHz	378M	458.752KHz	462MHz	672MHz	910MHz	924MHz	1.400GHz
15	180MHz	184.32MH	214.77MHz	240Mhz	360MHz	368.64MHz	375MHz	405M	491.52KHz	495MHz	720Mhz	975MHz	990MHz	1.500GHz
16	192MHz	196.608MI	229.088MHz	256MHz	384MHz	393.216MHz	400MHz	432M	524.288KHz	528MHz	768MHz	1.040GHz	1.056GHz	1.600GHz
17	204MHz	208.896MI	243.406MHz	272MHz	408MHz	417.792MHz	425MHz	459M	557.056KHz	561MHz	816MHz	1.105GHz	1.122GHz	1.700GHz
18	216MHz	221.184MI	257.724MHz	288MHz	432MHz	442.368MHz	450MHz	486M	589.824KHz	594MHz	864MHz	1.170GHz	1.188GHz	1.800GHz
19	228MHz	233.472MI	272.042MHz	304MHz	456MHz	466.944MHz	475MHz	513M	622.592KHz	627MHz	912MHz	1.235GHz	1.254GHz	1.900GHz
20	240MHz	245.76MH	286.36MHz	320MHz	480MHz	491.52MHz	500MHz	540M	655.36KHz	660MHz	960Mhz	1.300GHz	1.320GHz	2.000GHz
21	252MHz	258.048MI	300.678MHz	336MHz	504MHz	516.096MHz	525MHz	567M	688.128KHz	693MHz	1.008GHz	1.365GHz	1.386GHz	2.100GHz
22	264MHz	270.336MI	314.996MHz	352MHz	528MHz	540.672MHz	550MHz	594M	720.896KHz	726MHz	1.056GHz	1.430GHz	1.452GHz	2.200GHz
23	276MHz	282.624MI	329.314MHz	368MHz	552MHz	565.248MHz	575MHz	621M	753.664KHz	759MHz	1.104GHz	1.495GHz	1.518GHz	2.300GHz
24	288MHz	294.912MI	343.632MHZ	384MHz	576MHz	589.824MHz	600MHz	648M	786.432KHz	792MHz	1.152GHz	1.560GHz	1.584GHz	2.400GHz
25	300MHz	307.2MHz	357.95MHz	400MHz	600MHz	614.4MHz	625MHz	675M	819.2KHz	825MHz	1.200GHz	1.625GHz	1.650GHz	2.500GHz
26	312MHz	319.488MI	372.268MHz	416MHz	624MHz	638.976MHz	650MHz	702M	851.968KHz	858MHz	1.248GHz	1.690GHz	1.716GHz	2.600GHz
27	324MHz	331.776MI	386.586MHz	432MHz	648MHz	663.552MHz	675MHz	729M	884.736KHz	891MHz	1.296GHz	1.755GHz	1.782GHz	2.700GHz
28	336MHz	344.064MI	400.904MHz	448MHz	672MHz	688.128MHz	700MHz	756M	917.504KHz	924MHz	1.344GHz	1.820GHz	1.848GHz	2.800GHz
29	348MHz	356.352MI	415.222MHz	464MHz	696MHz	712.704MHz	725MHz	783M	950.272KHz	957MHZ	1.392GHz	1.885GHz	1.914GHz	2.900GHz
30	360MHz	368.64MH	429.54MHz	480MHz	720MHz	737.28MHz	750MHz	810M	983.04KHz	990MHz	1.440GHz	1.950GHz	1.980GHz	3.000GHz
31	372MHz	380.928MI	443.858MHz	496MHz	744MHz	761.856MHz	775MHz	837M	1.015MHz	.023GHz	1.488GHz	2.015GHz	2.046GHz	3.100GHz
32	384MHz	393.216MI	458.176MHz	512MHz	768MHz	786.432MHz	800MHz	864M	1.048MHz	.056GHz	1.536GHz	2.080GHz	2.112GHz	3.200GHz
33	396MHz	405.504MI	472.494MHz	528MHz	792MHz	811.008MHz	825MHz	891M	1.081MHz	.089GHz	1.584GHz	2.145GHz	2.178GHz	3.300GHz
34	408MHz	417.792MI	486.812MHz	544MHz	816MHz	835.584MHz	850MHz	918M	1.114MHz	.122GHz	1.632GHz	2.210GHz	2.244GHz	3.400GHz
35	420MHz	430.08MH	501.13MHz	560MHz	840MHz	860.16MHz	875MHZ	945M	1.146MHz	.155GHz	1.680GHz	2.275GHz	2.310GHz	3.500GHz
36	432MHz	442.368MI	515.448MHz	576MHz	864MHz	884.736MHz	900MHz	972M	1.179MHz	.188GHz	1.728GHz	2.340GHz	2.376GHz	3.600GHz
37	444MHz	45.656MH	529.766MHz	592MHz	888MHz	909.312MHz	925MHz	999M	1.212MHz	.221GHz	1.776GHz	2.405GHz	2.442GHz	3.700GHz
38	456MHz	466.944MI	544.084MHz	608MHz	912MHz	933.888MHz	950MHz	1026M	1.245MHz	.254GHz	1.824GHz	2.470GHz	2.508GHz	3.800GHz
39	468MHz	479.232MI	558.402MHz	624MHz	936MHz	958.464MHz	975MHz	1053M	1.277MHz	.287GHz	1.872GHz	2.535GHz	2.574GHz	3.900GHz
40	480MHz	491.52MH	572.72MHz	640MHz	960MHz	983.04MHz	1GHz	1080M	1.310MHz	.320GHz	1.920GHz	2.600GHz	2.640GHz	4.000GHz

1.4.5 Audio Performance

Digital Playback (PC-D-A) for Line Output

Test Items	Mobile System
Full Scale Output Voltage	≧0.7Vrms (3.3V audio)
Sample Frequency Accuracy	≦0.1%
Frequency Response (44.1ks/sec)	20Hz～15kHz
Frequency Response (48ks/sec)	20Hz～15kHz
Dynamic Range (SNR)	≧70dBFSA
THD+N	≦-55dBFS
Cross-talk	≧50dB

Analog Pass-Through (A-A) for Microphone Input to Line Outpu

Test Items	Mobile System
Frequency Response	100Hz～12kHz
Dynamic Range (SNR)	≧60dBFSA
THD+N	≦-50dBFS

Digital Recording (A-D-PC) for Microphone Input

Test Items	Mobile System
Full Scale Input Voltage	≧100mVrms
Sample Frequency Accuracy	≦0.1%
Frequency Response(22.05ks/sec)	100Hz～8.8kHz
Dynamic Range (SNR)	≧60dBFSA
THD+N	≦-50dBFS

Digital Recording (A-D-PC) for Microphone Input

Test Items	Mobile System
Full Scale Input Voltage	≧100mVrms
Sample Frequency Accuracy	≦0.1%
Frequency Response(22.05ks/sec)	100Hz～8.8kHz
Dynamic Range (SNR)	≧60dBFSA
THD+N	≦-50dBFS

1.5 APPENDIX

APPENDIX A WILLAMETTE CPU CORE FREQUENCY SELECTION

Bus Ratio	FSB400	FSB533	FSB800
1/16	1.60GHz	2.13GHz	3.2GHz
1/17	1.70GHz	2.26GHz	3.4GHz
1/18	1.80GHz	2.4GHz	3.6GHz
1/19	1.90GHz	2.53GHz	3.8GHz
1/20	2.00GHz	2.66GHz	RESERVED
1/21	2.10GHz	2.80GHz	RESERVED
1/22	2.20GHz	2.93GHz	RESERVED
1/23	2.30GHz	3.06GHz	RESERVED
1/24	2.40GHz	3.20GHz	RESERVED
1/26	2.5GHz	3.46GHz	RESERVED
1/28	2.6GHz	3.73GHz	RESERVED

APPENDIX B VOLTAGE IDENTIFICATION DEFINITION

VID4	VID3	VID2	VID1	VID0	VID5	VDAC
0	1	0	1	0	0	0.8375V
0	1	0	0	1	1	0.8500V
0	1	0	0	1	0	0.8625V
0	1	0	0	0	1	0.8750V
0	1	0	0	0	0	0.8875V
0	0	1	1	1	1	0.9000V
0	0	1	1	1	0	0.9125V
0	0	1	1	0	1	0.9250V
0	0	1	1	0	0	0.9375V
0	0	1	0	1	1	0.9500V
0	0	1	0	1	0	0.9625V
0	0	1	0	0	1	0.975V0
0	0	1	0	0	0	0.9875V
0	0	0	1	1	1	1.0000V
0	0	0	1	1	0	1.0125V
0	0	0	1	0	1	1.0250v
0	0	0	1	0	0	1.0375V
0	0	0	0	1	1	1.0500V
0	0	0	0	1	0	1.0625V
0	0	0	0	0	1	1.0750V
0	0	0	0	0	0	1.0875V
1	1	1	1	1	1	OFF
1	1	1	1	1	0	OFF
1	1	1	1	0	1	1.1000V
1	1	1	1	0	0	1.1125V
1	1	1	0	1	1	1.1250V
1	1	1	0	1	0	1.1375V
1	1	1	0	0	1	1.1500V
1	1	1	0	0	0	1.1625V
1	1	0	1	1	1	1.1750V
1	1	0	1	1	0	1.1875V
1	1	0	1	0	1	1.2000V
1	1	0	1	0	0	1.2125V
1	1	0	0	1	1	1.2250V

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1	1	0	0	1	0	1.2375V
1	1	0	0	0	1	1.2500V
1	1	0	0	0	0	1.2625V
1	0	1	1	1	1	1.2750V
1	0	1	1	1	0	1.2875V
1	0	1	1	0	1	1.3000V
1	0	1	1	0	0	1.3125V
1	0	1	0	1	1	1.3250V
1	0	1	0	1	0	1.3375V
1	0	1	0	0	1	1.3500V
1	0	1	0	0	0	1.3625V
1	0	0	1	1	1	1.3750V
1	0	0	1	1	0	1.3875V
1	0	0	1	0	1	1.4000V
1	0	0	1	0	0	1.4125V
1	0	0	0	1	1	1.4250V
1	0	0	0	1	0	1.4375V
1	0	0	0	0	1	1.4500V
1	0	0	0	0	0	1.4625V
0	1	1	1	1	1	1.4750V
0	1	1	1	1	0	1.4875V
0	1	1	1	0	1	1.5000V
0	1	1	1	0	0	1.5125V
0	1	1	0	1	1	1.5250V
0	1	1	0	1	0	1.5375V
0	1	1	0	0	1	1.5500V
0	1	1	0	0	0	1.5625V
0	1	0	1	1	1	1.5750V
0	1	0	1	1	0	1.5875V
0	1	0	1	0	1	1.6000V

APPENDIX C FREQUENCY TABLE FOR BCLK[1:0]

BSEL1	BSEL0	Function
L	L	100MHz
L	H	133MHz
H	L	200MHz
H	H	RSV

- **LCD CABLE REQUIREMENT**

  - Each differential pair need meet maximum impedance 100Ω

  - DC impedance have to meet maximum impedance 5mΩ in each line

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QDI QD141X1LH12 Cable pin define for one channel type

Signal name	M/B pin Number	LCD module pin number
LCDVCC	1	2
LCDVCC	2	3
GND	3	1
GND	4	10
GND	5	13
GND	6	16
TX2CLK+	7	
TXCLK+	8	18
TX2CLK-	9	
TXCLK-	10	17
GND	11	19
GND	12	
TX2OUT0+	13	
TX2OUT1+	14	
TX2OUT0-	15	
TX2OUT1-	16	
GND	17	
GND	18	
TX2OUT2+	19	
TXOUT0+	20	9
TX2OUT2-	21	
TXOUT0-	22	8
GND	23	
GND	24	
TXOUT2+	25	15
TXOUT1+	26	12
TXOUT2-	27	14
TXOUT1-	28	11
GND	29	
GND	30	
LCD_ID0	31	Link
+3VS	32	

8555 N/B Maintenance

QDI QD141X1LH12 Cable pin define for one channel type

Signal name	M/B pin Number	LCD module pin number
LCD_ID0	35	
+3VS	36	
LCD_ID0	37	
+3VS	38	
GND	39	
GND	40	

Note :

DISPLAY	Link Pin
QDI141X1LH12	31&32 Short

AU B141XN04-2 Cable pin define for one channel type

Signal name	M/B pin Number	LCD module pin number
LCDVCC	1	1
LCDVCC	2	2
GND	3	3
GND	4	4
GND	5	7
GND	6	10
TX2CLK+	7	
TXCLK+	8	15
TX2CLK-	9	
TXCLK-	10	14
GND	11	13
GND	12	16
TX2OUT0+	13	
TX2OUT1+	14	
TX2OUT0-	15	
TX2OUT1-	16	

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Signal name	M/B pin Number	LCD module pin number
GND	17	19
GND	18	20
TX2OUT2+	19	
TXOUT0+	20	6
TX2OUT2-	21	
TXOUT0-	22	5
GND	23	
GND	24	
TXOUT2+	25	12
TXOUT1+	26	9
TXOUT2-	27	11
TXOUT1-	28	8
GND	29	
GND	30	
LCD_ID0	31	
+3VS	32	
LCD_ID1	33	Link
+3VS	34	
LCD_ID0	35	
+3VS	36	
LCD_ID0	37	
+3VS	38	
GND	39	
GND	40	

Note :

DISPLAY	Link Pin
B141XN04-2	**33&34 Short**

8555 N/B Maintenance

CHI MEI N141X6-L01 Cable pin define for one channel type

Signal name	M/B pin Number	LCD module pin number
LCDVCC	1	1
LCDVCC	2	2
GND	3	3
GND	4	4
GND	5	7
GND	6	10
TX2CLK+	7	
TXCLK+	8	15
TX2CLK-	9	
TXCLK-	10	14
GND	11	13
GND	12	16
TX2OUT0+	13	
TX2OUT1+	14	
TX2OUT0-	15	
TX2OUT1-	16	
GND	17	19
GND	18	20
TX2OUT2+	19	
TXOUT0+	20	6
TX2OUT2-	21	
TXOUT0-	22	5
GND	23	
GND	24	
TXOUT2+	25	12
TXOUT1+	26	9
TXOUT2-	27	11
TXOUT1-	28	8
GND	29	
GND	30	
LCD_ID0	31	Link
+3VS	32	

8555 N/B Maintenance

Signal name	M/B pin Number	LCD module pin number
LCD_ID1	33	Link
+3VS	34	
LCD_ID0	35	
+3VS	36	
LCD_ID0	37	
+3VS	38	
GND	39	
GND	40	

Note :

DISPLAY	Link Pin
N141X6-L01	**31&32,33&34 Short**

HANNSTAR HSD150P-B LCD Cable pin define for one channel type

Signal name	M/B pin Number	LCD module pin number
LCDVCC	1	1
LCDVCC	2	2
GND	3	3
GND	4	4
GND	5	7
GND	6	10
TX2CLK+	7	
TXCLK+	8	15
TX2CLK-	9	
TXCLK-	10	14
GND	11	13
GND	12	16
TX2OUT0+	13	
TX2OUT1+	14	
TX2OUT0-	15	
TX2OUT1-	16	

8555 N/B Maintenance

Signal name	M/B pin Number	LCD module pin number
GND	17	19
GND	18	20
TX2OUT2+	19	
TXOUT0+	20	6
TX2OUT2-	21	
TXOUT0-	22	5
GND	23	
GND	24	
TXOUT2+	25	12
TXOUT1+	26	9
TXOUT2-	27	11
TXOUT1-	28	8
GND	29	
GND	30	
LCD_ID0	31	
+3VS	32	
LCD_ID1	33	
+3VS	34	
LCD_ID0	35	Link
+3VS	36	
LCD_ID0	37	
+3VS	38	
GND	39	
GND	40	

Note :

DISPLAY	Link Pin
HSD150PX11-B	35&36 Short

8555 N/B Maintenance

HYUNDAI HT15X31-100 LCD Cable pin define for one channel type

Signal name	M/B pin Number	LCD module pin number
LCDVCC	1	1
LCDVCC	2	2
GND	3	3
GND	4	4
GND	5	7
GND	6	10
TX2CLK+	7	
TXCLK+	8	15
TX2CLK-	9	
TXCLK-	10	14
GND	11	13
GND	12	16
TX2OUT0+	13	
TX2OUT1+	14	
TX2OUT0-	15	
TX2OUT1-	16	
GND	17	19
GND	18	20
TX2OUT2+	19	
TXOUT0+	20	6
TX2OUT2-	21	
TXOUT0-	22	5
GND	23	
GND	24	
TXOUT2+	25	12
TXOUT1+	26	9
TXOUT2-	27	11
TXOUT1-	28	8
GND	29	
GND	30	
LCD_ID0	31	Link
+3VS	32	

8555 N/B Maintenance

HYUNDAI HT15X31-100 LCD Cable pin define for one channel type

Signal name	M/B pin Number	LCD module pin number
LCD_ID1	33	
+3VS	34	
LCD_ID0	35	Link
+3VS	36	
LCD_ID0	37	
+3VS	38	
GND	39	
GND	40	

Note :

DISPLAY	Link Pin
HT15X31-100	**31&32,35&36 Short**

AU B150PG01 LCD Cable pin define for two channel type

Signal name	M/B pin Number	LCD module pin number
LCDVCC	1	2
LCDVCC	2	3
GND	3	1
GND	4	10
GND	5	13
GND	6	16
TX2CLK+	7	30
TXCLK+	8	18
TX2CLK-	9	29
TXCLK-	10	17
GND	11	19
GND	12	22
TX2OUT0+	13	21
TX2OUT1+	14	24

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Signal name	M/B pin Number	LCD module pin number
TX2OUT0-	15	20
TX2OUT1-	16	23
GND	17	25
GND	18	28
TX2OUT2+	19	27
TXOUT0+	20	9
TX2OUT2-	21	26
TXOUT0-	22	8
GND	23	
GND	24	
TXOUT2+	25	15
TXOUT1+	26	12
TXOUT2-	27	14
TXOUT1-	28	11
GND	29	
GND	30	
LCD_ID0	31	
+3VS	32	
LCD_ID1	33	Link
+3VS	34	
LCD_ID0	35	Link
+3VS	36	
LCD_ID0	37	
+3VS	38	
GND	39	
GND	40	

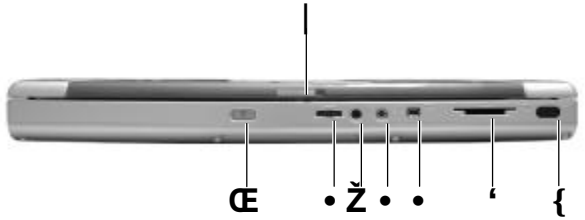
Note :

DISPLAY	Link Pin
B150PG01	33&34,35&36 Short

2. System View and Disassembly

2.1 System View

2.1.1 Front View



❶ Hold Switch
❷ Volume Control
❸ Audio Output
❹ Microphone Input
❺ 1394 port
❻ Card Reader Slot
❼ IR Module
❽ Top Cover Latch

2.1.2 Left-side View

❶ PCMCIA Card Socket
❷ CD/DVD-ROM Drive
❸ RJ-11 Connector
❹ RJ-45 Connector
❺ USB Port*2

2.1.3 Right-side View

❶ Kensington Lock
❷ Ventilation Openings
❸ Battery pack

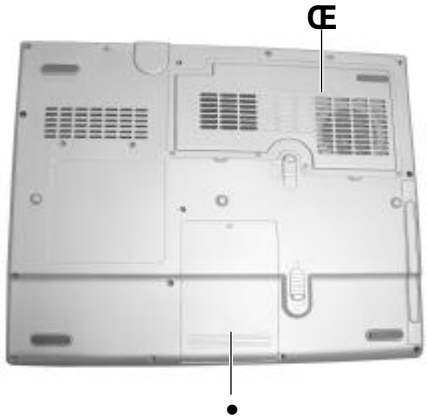
2.1.4 Rear View

❶ USB Port*2
❷ VGA Port
❸ S-Video Output Connector
❹ Parallel Port
❺ Power Connector

8555 N/B Maintenance

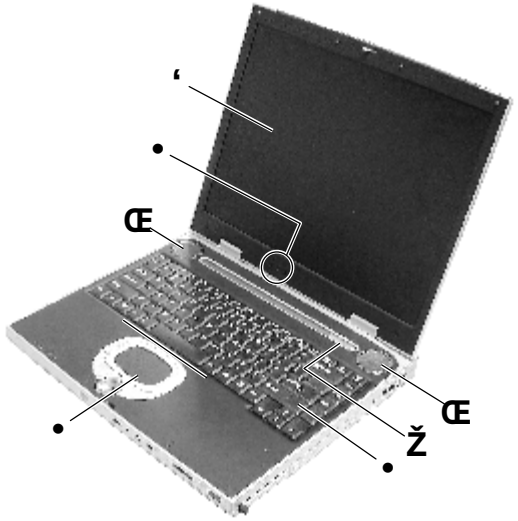
2.1.5 Bottom View

❶ CPU Cover
❷ Hard Disk Drive Cover



2.1.6 Top View

❶ Stereo Speaker
❷ Touch Pad
❸ Power Button
❹ Keyboard
❺ Device Indicators
❻ LCD Screen

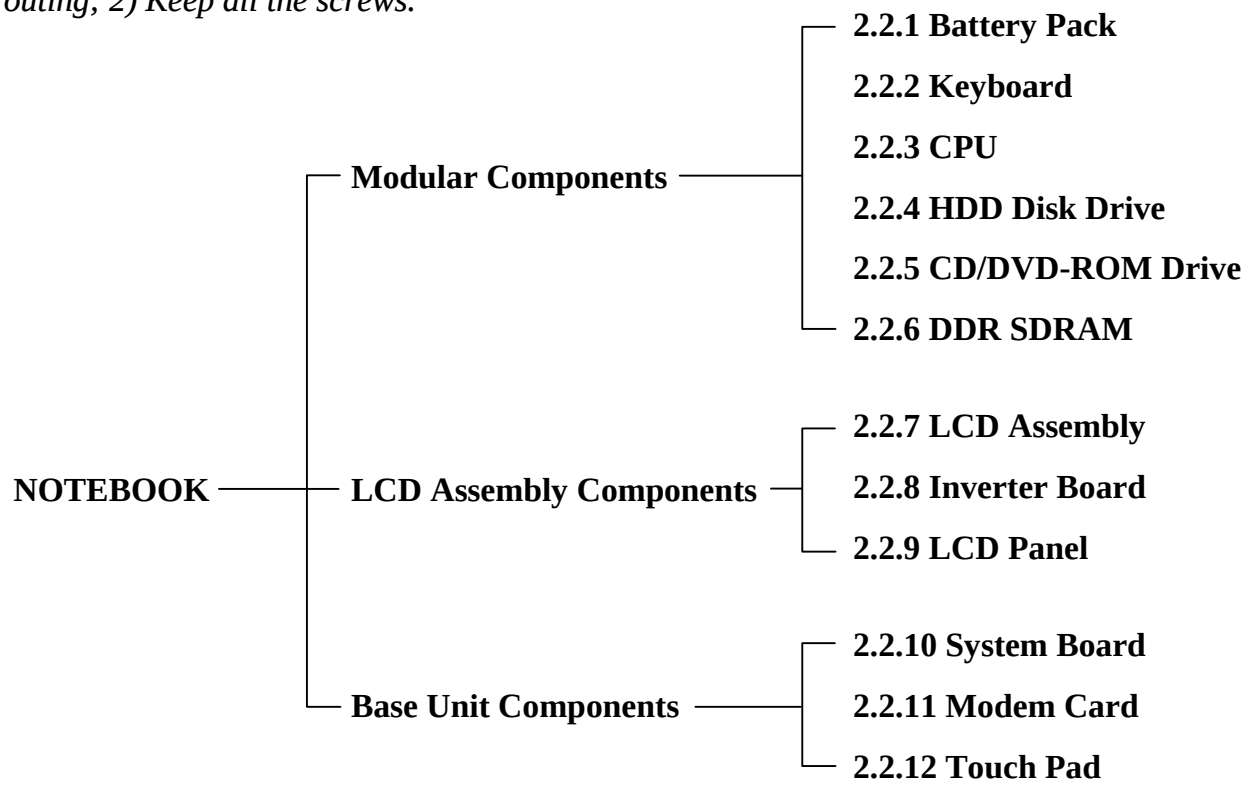


2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *1. Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*

2. During disassembly, 1) Label each cable as you disconnect it, noting its position and routing; 2) Keep all the screws.



2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide and keep the upper release lever on "unlock" (🔓) position (Œ), and then pull the battery pack out of the compartment (•) while sliding the lower release lever downwards to "unlock" (🔓) position (•). (Figure 2-1).

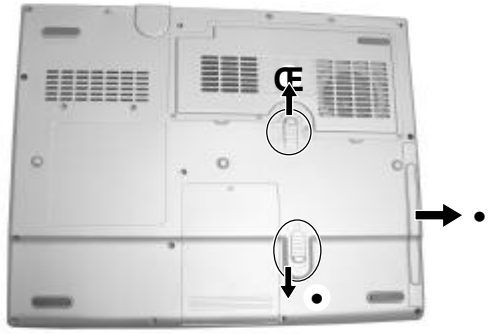


Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" (🔒) position.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (See section 2.2.1 Disassembly)
2. Remove three screws that fastening the keyboard cover on the bottom of the notebook. (Figure 2-2)

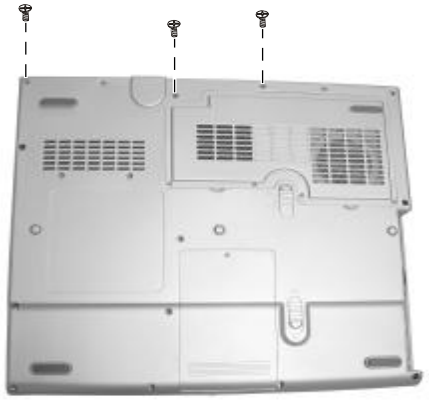


Figure 2-2 Remove three screws

Figure 2-3 Slide out the keyboard cover

3. Open the top cover. Slide out the keyboard cover. (Figure 2-3)

4. Remove two screws fastening the keyboard. (Figure 2-4)
5. Disconnect the cable from system board. (Figure 2-5)

Figure 2-4 Remove two screws

Figure 2-5 Disconnect the cable

Reassembly

1. Reconnect the keyboard cable.
2. Replace the keyboard and secure with two screws.
3. Replace the keyboard cover and secure with three screws.
4. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.3 CPU

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove four screws that fasten the heatsink compartment covers. (Figure 2-6)

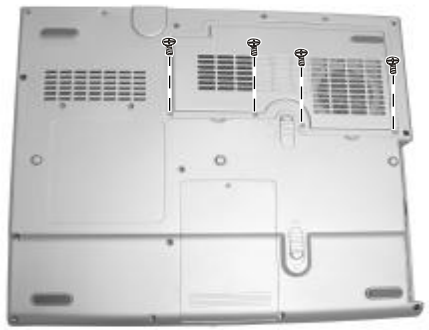


Figure 2-6 Remove four screws

Figure 2-7 Remove the heatsink compartment cover

4. Remove four spring screws fastening the heatsink. (Figure 2-7)

5. Disconnect the fan's power cord to detach the heatsink from the CPU compartment. (Figure 2-8)
6. To remove the existing CPU, lift the socket arm up to the vertical position. (Figure 2-9)

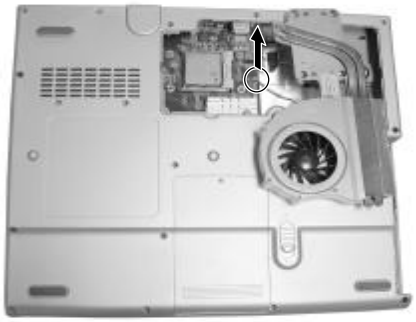


Figure 2-8 Disconnect the fan's cord

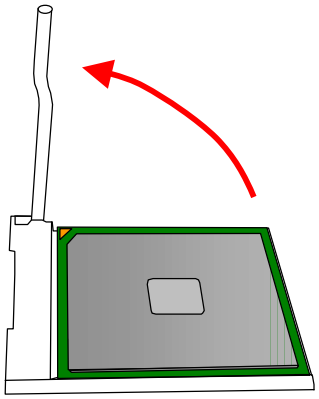


Figure 2-9 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Place the lever back to the horizontal position and push the lever to the left .
2. Connect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with four spring screws.
3. Replace the heatsink compartment cover and secure with four screws.
4. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove one screw fastening the HDD compartment cover. Then sliding it outward. (Figure 2-10)

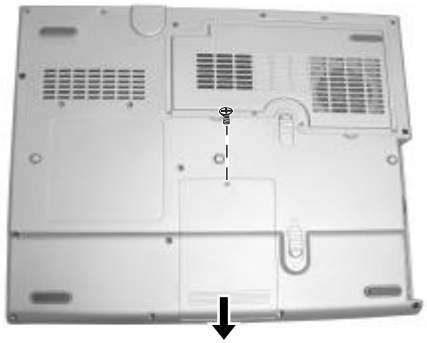


Figure 2-10 Remove HDD compartment cover

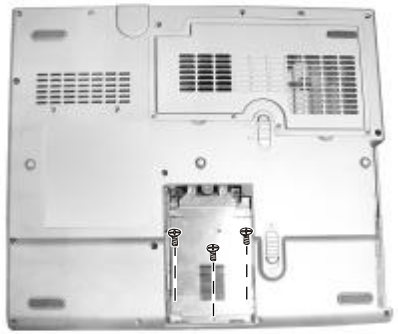


Figure 2-11 Remove three screws that secure the top shielding

4. Remove three screws that secure the top shielding of the hard disk drive. (Figure 2-11)

5. Unscrew two screws to slide out the hard disk drive from the compartment. (Figure 2-12)

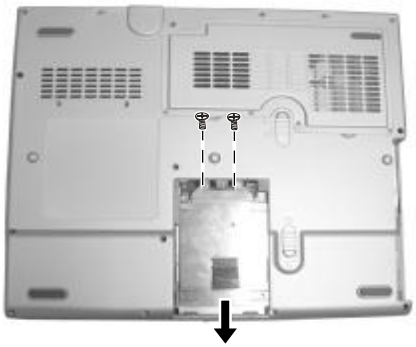


Figure 2-12 slide out the hard disk drive

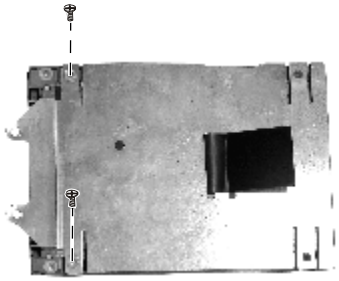


Figure 2-13 Free the hard disk

6. To free the hard disk drive, remove two screws that secure the holding. (Figure 2-13)

Reassembly

1. Fit the hard disk drive into the holding and secure with two screws.
2. Replace the hard disk drive into compartment and secure with two screws.
3. Fit the top shielding and secure with three screws.
4. Replace the HDD's cover and secure with one screw.
5. Then replace battery pack. (See section 2.2.1 Reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove three screws fastening the CD/DVD-ROM drive. (Figure 2-12)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (Œ) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out(•). (Figure 2-14)

Figure 2-14 Remove the CD/DVD -ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with three screws.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.6 SO-DIMM

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack and the keyboard. (See sections 2.2.1and 2.2.2 disassembly)
2. Pull the retaining clips outwards (Œ) and remove the SO-DIMM (•). (Figure 2-15)

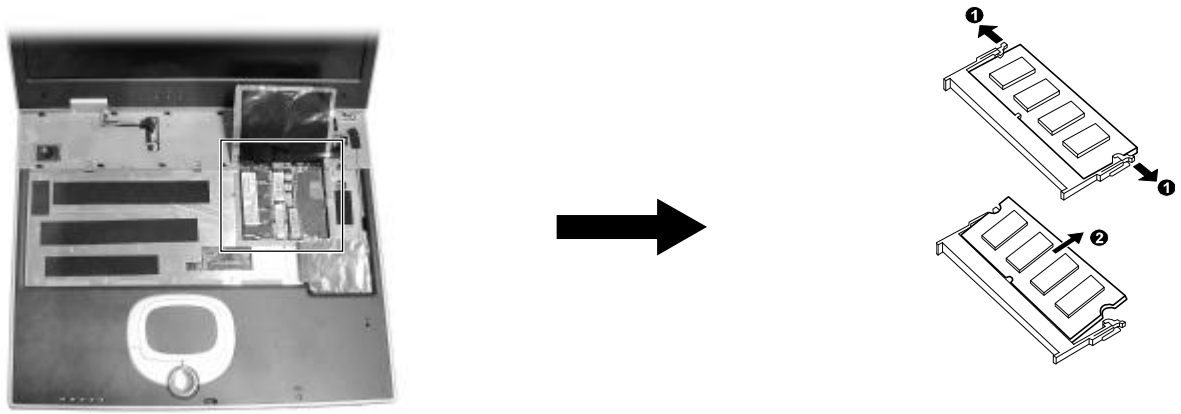


Figure 2-15 Remove the SO-DIMM

Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace the battery pack and the keyboard. (See sections 2.2.1 and 2.2.2 reassembly)

2.2.7 LCD Assembly

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack and the keyboard. (See sections 2.2.1and 2.2.2 disassembly)
2. Remove two screws on the rear side of notebook. (Figure 2-16)
3. Open the top cover. Rip the insulating tape off to free the antenna. (Figure 2-17)

Figure 2-16 Remove two screws

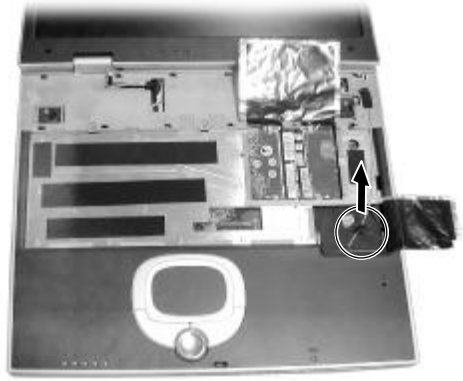


Figure 2-17 Free the antenna

6. Then remove the two hinge covers. (Figure 2-18)
7. Remove two screws of the hinges. And disconnect the two LCD wires from the system board. (Figure 2-19)

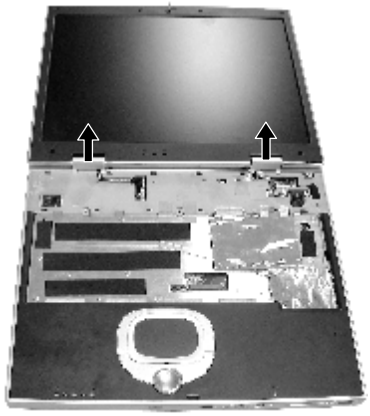


Figure 2-18 Remove the hinge cover

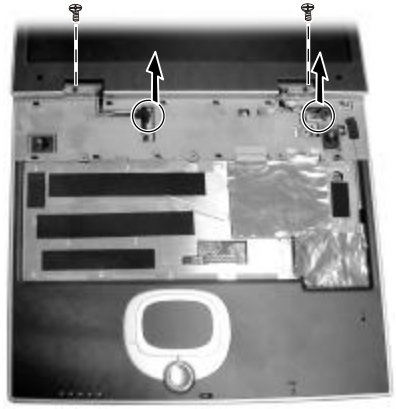


Figure 2-19 Disconnect the two LCD wires

8. Carefully put the notebook upside down, remove two screws of the hinges. Now you can separate the LCD assembly from the base unit. (Figure 2-20)

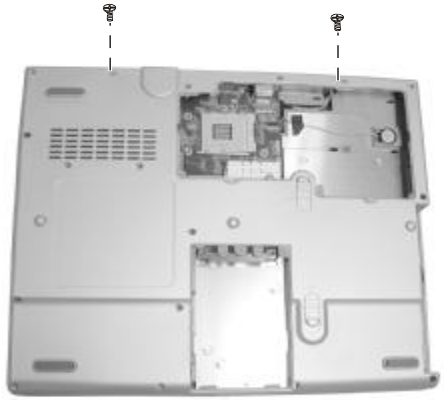


Figure 2-20 Remove the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws of the hinges.
2. Reconnect the LCD wires to the system board..
3. Fit two hinge covers and secure with two screws.
4. Replace the battery pack and the keyboard. (See section 2.2.1 and 2.2.2 reassembly) .

2.2.8 Inverter Board

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack and the keyboard. (See sections 2.2.1and 2.2.2 disassembly)
2. Remove the LCD Assembly. (See section 2.2.7 Disassembly)
3. Remove the four rubber pads and four screws. (figure 2-21)
4. Insert a flat screwdriver to the lower part of the top cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
5. Disconnect one wire from inverter board and remove two screws fastening the inverter board. (Figure 2-22)

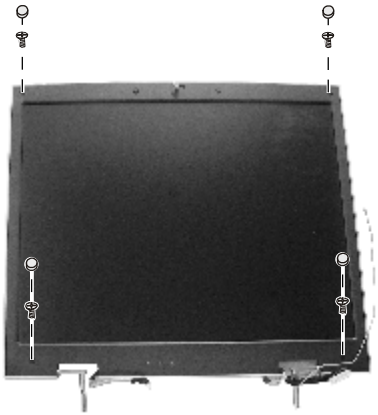


Figure 2-21 Unscrew four screws

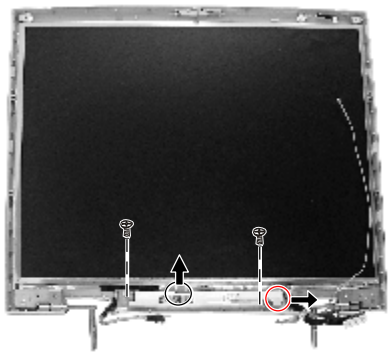


Figure 2-22 Disconnect one cables

Reassembly

1. Fit the inverter board back into place and secure with two screws, and reconnect the wire to the inverter board.
2. Fit the LCD top cover back into the housing and secure with four screws and four rubber pads
3. Replace the LCD Assembly. (See section 2.2.7 Reassembly)
4. Replace the battery pack and the keyboard. (See section 2.2.1 and 2.2.2 reassembly) .

2.2.9 LCD Panel

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the LCD Assembly. (See section 2.2.7 Disassembly)
4. Disconnect one wire from inverter board and remove two screws fastening the inverter board. (Figure 2-23)
5. Remove eight screws. And then lift up LCD panel. (Figure 2-23)
6. To free the LCD panel, remove eight screws. (Figure 2-24)

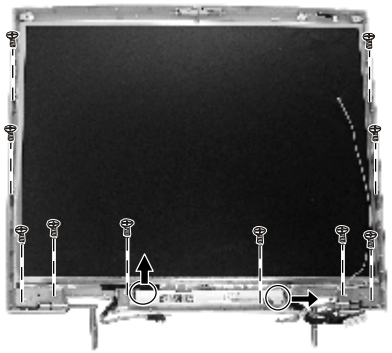


Figure 2-23 Separate the LCD panel

Figure 2-24 Unscrew eight screws

Reassembly

1. Attach the LCD panel holding to panel and secure with eight screws.
2. Fit the LCD panel into place and secure with eight screws.
3. Replace the inverter board. (See section 2.2.8 Reassembly)
4. Replace the LCD assembly. (See section 2.2.7 Reassembly)
5. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.10 System Board

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR-SDRAM and LCD Assembly. (See the previous sections Disassembly)
4. Remove nine screws on the bottom of notebook. (Figure 2-25)
5. Turnover the notebook. Remove two screws. And disconnect three wires. (Figure 2-26)

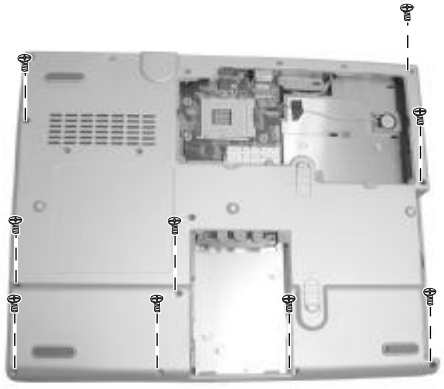


Figure 2-25 Unscrew nine screws

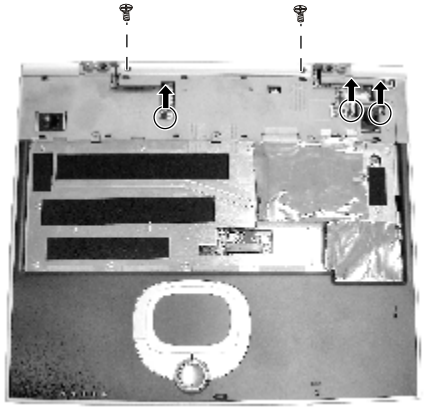


Figure 2-26 Remove two screws

6. Disconnect the touch pad's cable. Then lift up the system top cover. (Figure 2-27)

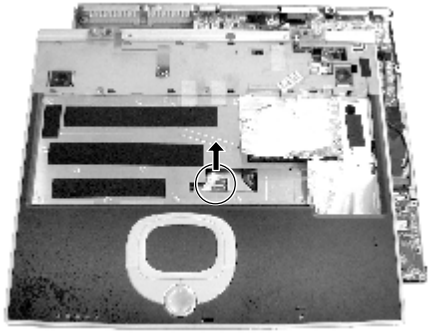


Figure 2-27 Remove the top cover

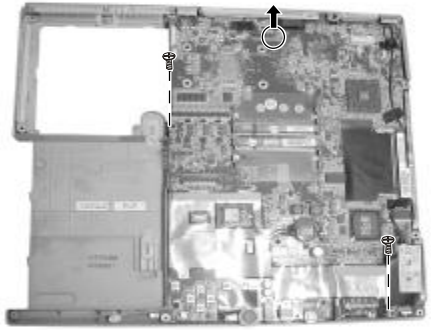


Figure 2-28 Unscrew two screws and disconnect one cord

7. Unscrew two screws and disconnect fan's cord. (Figure 2-28)

8. Remove four hex nuts beside the VGA ports. Now you can lift up system board from housing. (Figure 2-29)

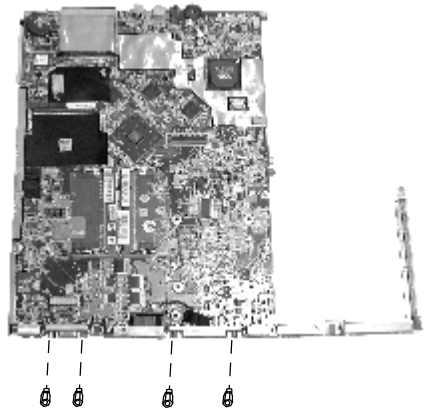


Figure 2-29 Remove four hex nuts

Reassembly

1. Fit the system board back into housing and secure with two screws and four hex nuts.
2. Reconnect the fan's cord.
3. Fit the top cover. Reconnect the touch pad's cable to system board.
4. Reconnect the speaker's cords to system board.
5. Fasten the top cover by two screws.
6. Up the notebook upside down. Reconnect the other speaker's cord.
7. Fasten the housing by nine screws.
8. Reassemble the notebook. (See the previous sections Reassembly)

2.2.11 Modem Card

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR-SDRAM and LCD Assembly. (See the previous sections Disassembly)
4. Remove the system top cover. (See the steps1 to 6 of section 2.2.10 Disassembly)
5. Remove two screws fastening the modem card. disconnect cord from system board. (Figure 2-30)

Figure 2-30 Remove the modem card

Reassembly

1. Reconnect the cord. Then fit the modem card and secure with two screws.
2. Reassemble the notebook. (See the previous sections Reassembly)

2.2.12 Touch Pad

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR-SDRAM and LCD Assembly. (See the previous sections Disassembly)
4. Remove the system top cover. (See the steps1 to 6 of section 2.2.10 Disassembly)
5. Remove two screws fastening the touch pad bracket. Then remove it. (Figure 2-31)
6. Remove the click holder and touch pad panel. (Figure 2-31)

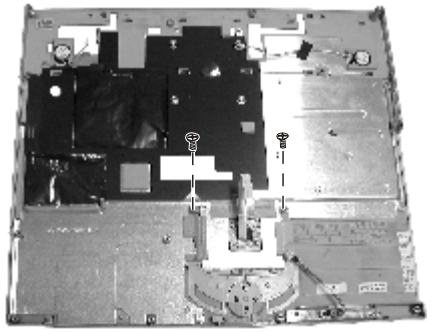


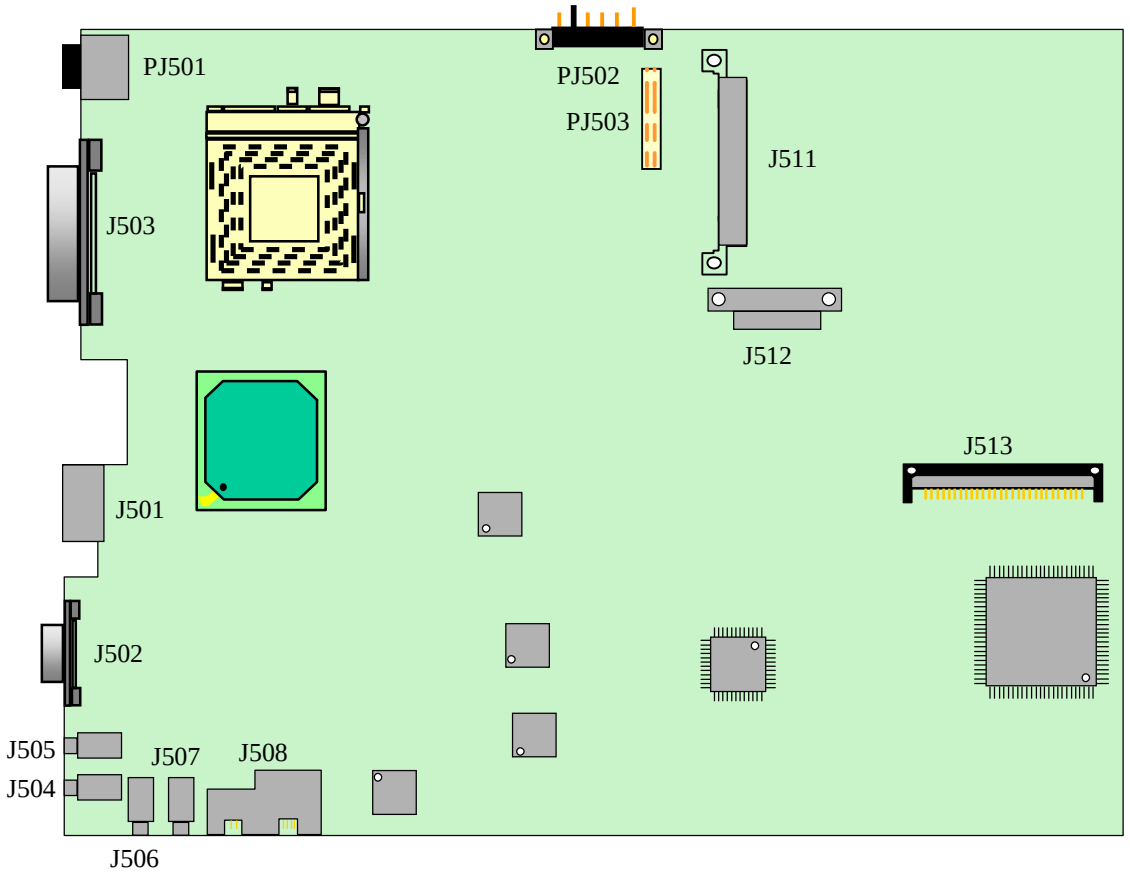
Figure 2-31 Free the touch pad

Reassembly

1. Fit the touch pad panel and click holder
2. Then fit the touch pad bracket and secure with two screws.
3. Reassemble the notebook. (See the previous sections Reassembly)

3. Definition & Location of Connectors / Switches

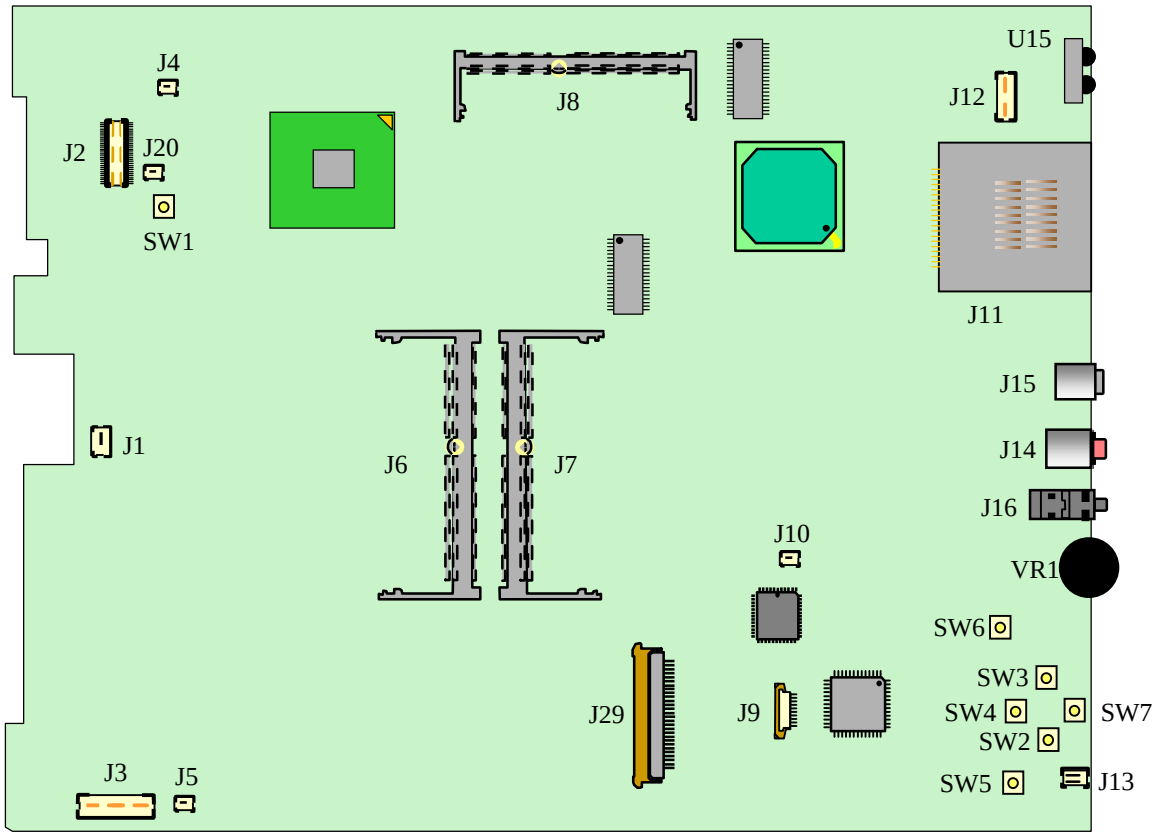
3.1 Mother Board-A



- **J501 : S-Video Connector**
- **J502 : VGA Connector**
- **J503 : Parallel Port**
- **J504 : USB2.0 Connector**
- **J505 : USB2.0 Connector**
- **J506 : USB2.0 Connector**
- **J507 : USB2.0 Connector**
- **J508 : RJ45 & RJ11 Connector**
- **J511 : Primary IDE HDD Connector**
- **J512 : Secondary IDE CD-ROM Connector**
- **J513 : PCMCIA Connector**
- **PJ502 : Battery Connector**
- **PJ503 : Charge Board Connector**

3. Definition & Location of Connectors / Switches

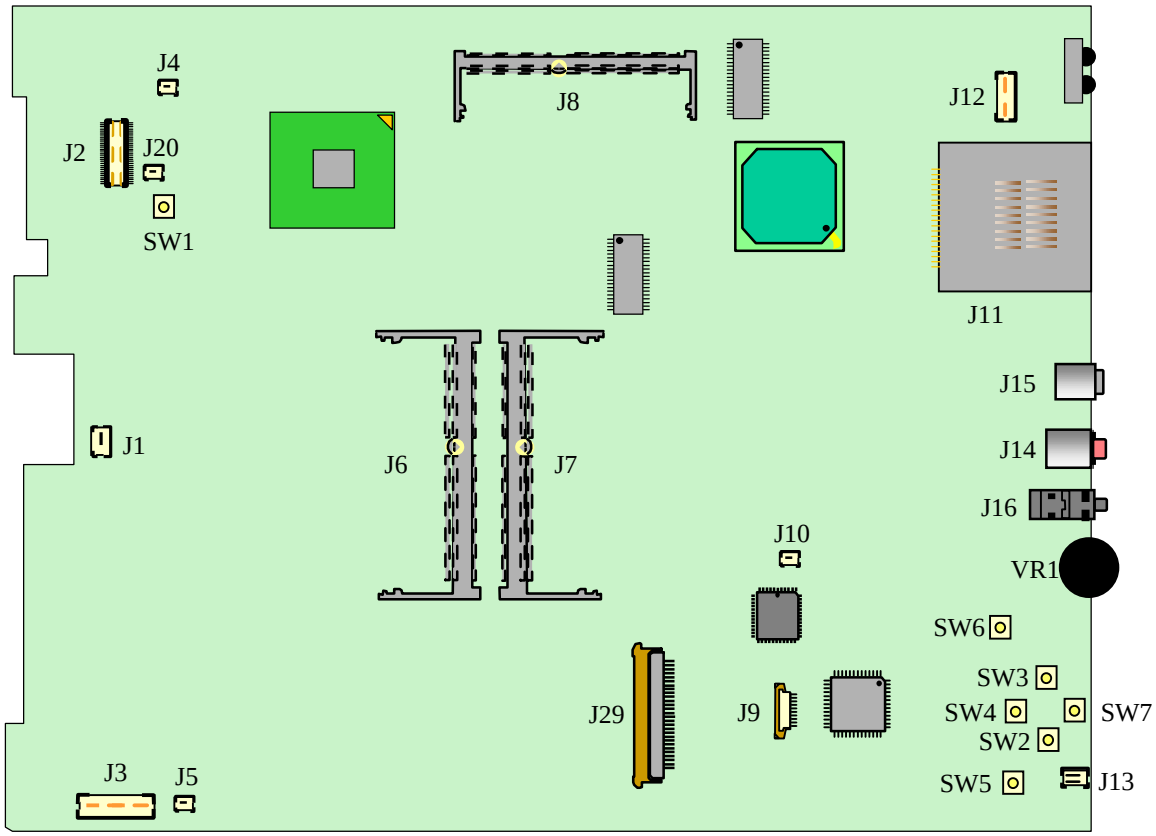
3.2 Mother Board-B



- J1 : CPU FAN Connector
- J2 : LCD Connector
- J3 : Invert Board Connector
- J4 : MDC Jump wire Connetor
- J5 : Left Speak Connector
- J6 : DDR Memory Connector
- J7 : DDR Memory Connector
- J8 : Mini PCI Connector
- J9 : Touch Pad Connector
- J10 : RTC Battery Connector
- J11 : SD Card Connector
- J12 : MDC Connector
- J13 : LED Board Connector
- J14 : Microphone Jack

3. Definition & Location of Connectors / Switches

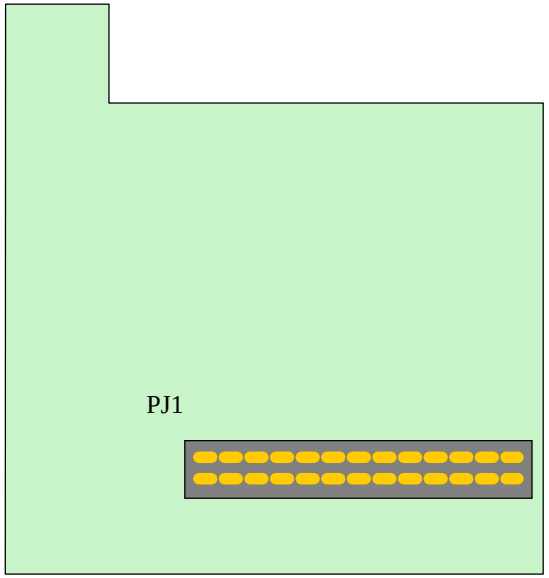
3.2 Mother Board-B



- **J15 : Mini 1394 Connector**
- **J16 : Line Out**
- **J20 : Right Speak Connector**
- **J29 : K/B Connector**
- **VR1 : Volume Control**
- **SW1 : Power Button**
- **SW2 : Left Scroll Button**
- **SW3 : Right Scroll Button**
- **SW4 : Up Scroll Button**
- **SW5 : Left Button**
- **SW6 : Right Button**
- **SW7 : Down Scroll Button**

3. Definition & Location of Connectors / Switches

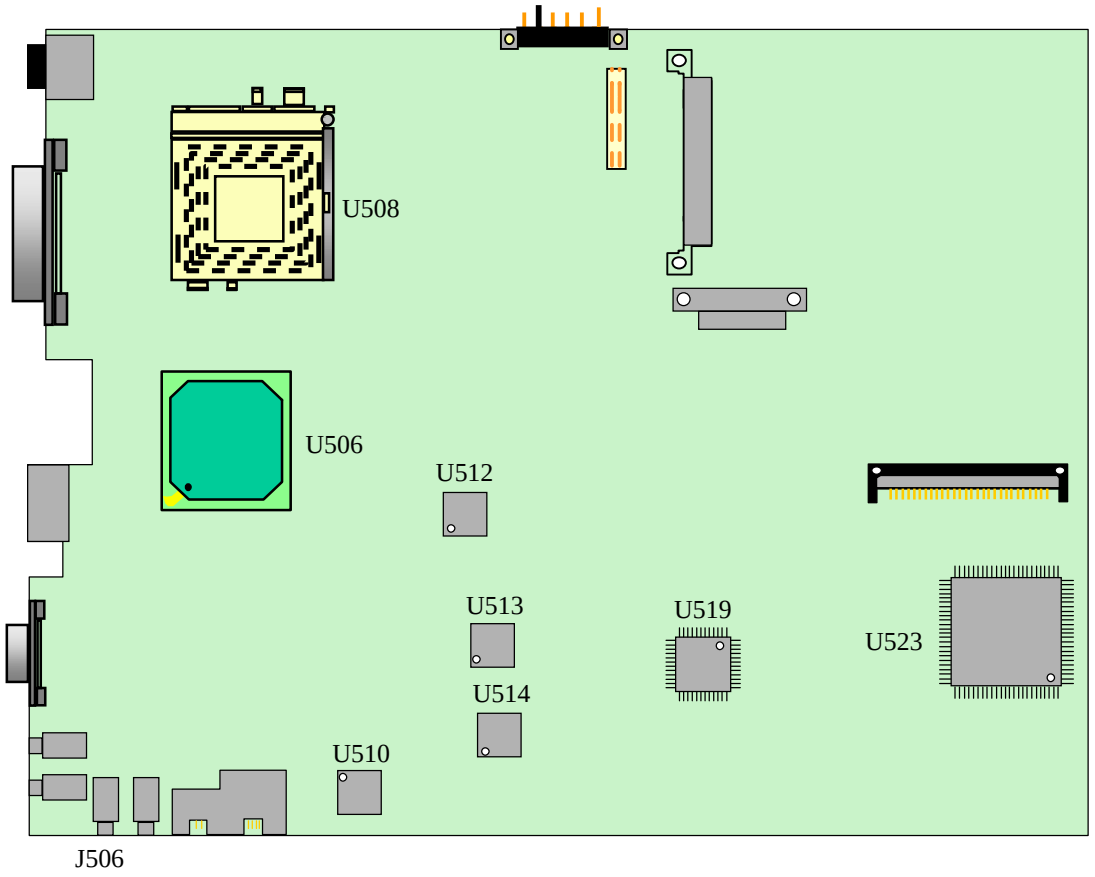
3.3 Charge Board



- **PJ1 : M/B Connector**

4. Definition & Location of Major Components

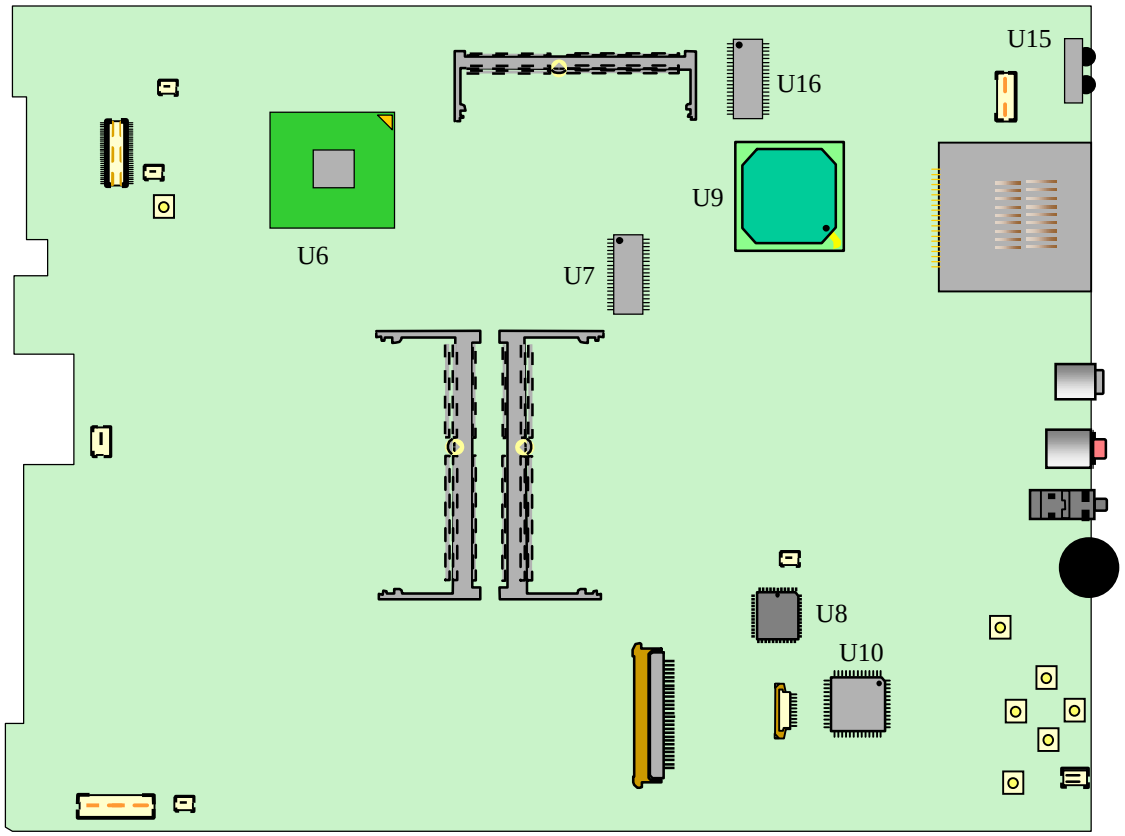
4.1 Mother Board-A



- **U506 : SiS648FX North Bridge**
- **U508 : CPU Socket**
- **U510 : HY5DU2832222F Video Memory**
- **U512 : HY5DU2832222F Video Memory**
- **U513 : HY5DU2832222F Video Memory**
- **U514 : HY5DU2832222F Video Memory**
- **U519 : PC87393 Super I/O Controller**
- **U523 : ENE CB710 CARDBUS Controller**

4. Definition & Location of Major Components

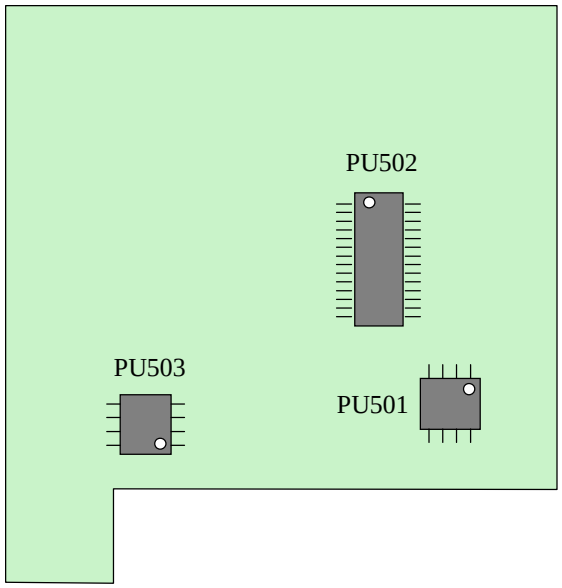
4.2 Mother Board-B



- **U6 : ATI M9+X Video Controller**
- **U7 : ICS952011 Clock Generator**
- **U8 : 28F020-PLCC BIOS**
- **U9 : SiS963 South Bridge**
- **U10 : H8/3437S**
- **U15 : FIR**
- **U16 : ICS1893AF**

4. Definition & Location of Major Components

4.3 Charge Board



- **PU501 : FDS77664A**
- **PU502 : Max1772**
- **PU503 : SI4410DY**

5. Pin Descriptions of Major Components

5.1 Mobile Prescott Northwood 533MHZ

Name	Type	Description
AP[1:0]#	Input/ Output	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#,A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus agents. The following table defines **Request Signals / subphase 1 / subphase 2** **A[35:24]# / AP0# / AP1#** **A[23:3]# / AP1# / AP0#** **REQ[4:0]# / AP1# / AP0#**
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V CROSS .
BINIT#	Input/ Output	BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Name	Type	Description
A[35:3]#	Input/ Output	A[35:3]# (Address) define a 2 36 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Pentium 4 processor in the 478-pin package system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration. See Section 7.1 for more details.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals / Associated Strobe** **REQ[4:0]#, A[16:3]# / ADSTB0#** **A[35:17]# / ADSTB1#**

5.1 Mobile Prescott Northwood 533MHZ

Name	Type	Description
BPM[5:0]#	Input/ Output	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor. Please refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more detailed information. **These signals do not have on-die termination. Refer to Section 2.5, the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for termination requirements.**
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	Input/ Output	BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this pin is sampled to determine the agent ID = 0. **This signal does not have on-die termination and must be terminated.**
BSEL[1:0]	Output	The BCLK[1:0] frequency select signals BSEL[1:0] are used to select the processor input clock frequency. Table 4 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The Pentium 4 processor in the 478-pin package operates currently at a 400 MHz system bus frequency (100 MHz BCLK[1:0] frequency). For more information about these pins, including termination recommendations refer to Section 2.9 and the appropriate platformdesign guidelines.
COMP[1:0]	Analog	COMP[1:0] must be terminated on the system board using precision resistors. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for details on implementation.

Name	Type	Description
D[63:0]#	Input/ Output	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DBI#. **Quad-Pumped Signal Groups** **Data Group / DSTBN#/ DSTBP# / DBI#** **D[15:0]# — 0 — 0** **D[31:16]# — 1 — 1** **D[47:32]# — 2 — 2** **D[63:48]# — 3 — 3** Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBI[3:0]#	Input/ Output	DBI[3:0]# are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DBI[3:0] Assignment To Data Bus** **Bus Signal / Data Bus Signals** **DBI3# — D[63:48]#** **DBI2# — D[47:32]#** **DBI1# — D[31:16]#** **DBI0# — D[15:0]#**
DBR#	Output	DBR# is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.

5.1 Mobile Prescott Northwood 533MHZ

Name	Type	Description
HIT# **HITM#**	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#. **This signals does not have on-die termination. Refer to Section 2.5 fortermination requirements.**
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error.IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
ITPCLKOUT[1:0]	Output	The ITPCLKOUT[1:0] pins do not provide any output for the Pentium® 4 processor in the 478-pin package. Refer to Section 2.5 for additional details and termination requirements.
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.

Name	Type	Description
DBSY#	Input/ Output	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus isreleased after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.
DEFER#	Input	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor system bus agents.
DP[3:0]#	Input/ Output	DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus gents.
DSTBN[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe D[15:0]#, DBI0# — DSTBN0# D[31:16]#, DBI1# — DSTBN1# D[47:32]#, DBI2# — DSTBN2# D[63:48]#, DBI3# — DSTBN3#
DSTBP[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe D[15:0]#, DBI0# — DSTBP0# D[31:16]#, DBI1# — DSTBP1# D[47:32]#, DBI2# — DSTBP2# D[63:48]#, DBI3# — DSTBP3#
FERR#	Output	FERR# (Floating-point Error) is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MSDOS*-type floating-point error reporting.
GTLREF	Input	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CC}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more information.

5.1 Mobile Prescott Northwood 533MHZ

Name	Type	Description
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Figure 11 illustrates the relationship of PWRGOOD to the RESET# signal. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 16, and be followed by a 1 to 10 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after VCC and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 7.1. **This signal does not have on-die termination and must be terminated on the system board.**
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.

Name	Type	Description
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: Enabled or disabled. Asserted, if configured, for internal errors along with IERR#. Asserted, if configured, by the request initiator of a bus transaction after it observes an error. Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, please refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*.
PROCHOT#	Output	PROCHOT# will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. See Section 7.3 for more details.

5.1 Mobile Prescott Northwood 533MHZ

Name	Type	Description
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for a details on parity checking of these signals.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If the BCLK input is stopped while in the Sleep state the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also knownas the Test Access Port).

Name	Type	Description
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[12:8] **TESTHI[5:0]**	Input	TESTHI[12:8] and TESTHI[5:0] must be connected to a VCC power source through a resistor for proper processor operation. See Section 2.5 for more details.
THERMDA	Other	Thermal Diode Anode. See Section 7.3.1.
THERMDC	Other	Thermal Diode Cathode. See Section 7.3.1.
THERMTRIP#	Output	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C.Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (VCC) must be removed following the assertion of THERMTRIP#. See Figure 12 and Table 16 for the appropriate power down sequence and timing requirements. Once activated, THERMTRIP# remains latched until RESET# is asserted. While the assertion of the RESET# signal will de-assert THERMTRIP# , if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted after RESET# is de-asserted.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 . pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.

5.1 Mobile Prescott Northwood 533MHZ

Name	Type	Description
VCCIOPLL	Input	VCCIOPLL provides isolated power for internal processor system bus PLLs. Follow he guidelines for VCCA, and refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel ® 850 Chipset Platform Design Guide* for complete implementation details.
VCCSENSE	Output	VCCSENSE is an isolated low impedance connection to processor core power(VCC). It can be used to sense or measure power near the silicon with little noise.
VCCVID	Input	There is no imput voltage requirement for VCCVID for designs intended tosupport only the Pentium 4 processor in the 478-pin package. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more information.
VID[4:0]	Output	VID[4:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages (Vcc). These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support processor voltage specification variations. See Table 2 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
VSSA	Input	VSSA is the isolated ground for internal PLLs.
VSSSENSE	Output	VSSSENSE is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 . pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.

5.2 SiS M661/648FX North Bridge

Host Bus Interface(1)

Pin Name	Pin Attr	Description
CPUCLK CPUCLK#	I 0.71V – M	Host differential clock input.
CPURST#	O 0.9~1.75V – M	Host Bus Reset: CPURST# is used to keep all the bus agents in the same initial state before valid cycles issued.
CPUPWRGD	O 0.9~1.75V – M	CPUPWRGD is used to inform CPU that main power is stable
ADS#	I/O 0.9~1.75V – M	Address Strobe : Address Strobe is driven by CPU or SiS648FX to indicate the start of a CPU bus cycle.
HADSTB[1:0]#	I/O 0.9~1.75V – M	Source synchronous address strobe used to latch HREQ[4:0]# & HA[31:3]# at both falling and rising edge. HREQ[4:0]# & HA[16:3]# are latched by HASTB0# HA[31:17] are latched by HASTB1#
HREQ[4:0]#	I/O 0.9~1.75V – M	Request Command: HREQ[4:0]# are used to define each transaction type during the clock when ADS# is asserted and the clock after ADS# is asserted.
HA[31:3]#	I/O 0.9~1.75V – M	Host Address Bus
BREQ0#	O 0.9~1.75V – M	Symmetric Agent Bus Request: BREQ0# is driven by the symmetric agent to request for the bus.
BPRI#	O 0.9~1.75V – M	Priority Agent Bus Request: BPRI# is driven by the priority agent that wants to request the bus. BPRI# has higher priority than BREQ0# to access a bus.
BNR#	I/O 0.9~1.75V – M	Block Next Request: This signal can be driven asserted by any bus agent to block further requests being pipelined.
DBI[3:0]#	I/O 0.9~1.75V – M	Dynamic Bus Inversion: An active DBI# will invert it's corresponding data group signals. DBI0# is referenced by HD[15:0], DBI1# is referenced by HD[31:16] DBI2# is referenced by HD[47:32] DBI3# is referenced by HD[63:48]
HLOCK#	I 0.9~1.75V – M	Host Lock : CPU asserts HLOCK# to indicate the current bus cycle is locked.

Host Bus Interface(2)

Pin Name	Pin Attr	Description
HIT#	I/O 0.9~1.75V – M	Keeping a Non-Modified Cache Line
HITM#	I/O 0.9~1.75V – M	Hits a Modified Cache Line: Hit Modified indicates the snoop cycle hits a modified line in the L1/L2 cache of CPU.
DEFER#	O 0.9~1.75V – M	Defer Transaction Completion: SiS648FX will use this signal to indicate a retry or defer response to host bus.
RS[2:0]#	O 0.9~1.75V – M	Response Status: RS[2:0]# are driven by the response agent to indicate the transaction response type. The following shows the response type. RS[2:0] Response 000 Idle State 001 Retry 010 Defer 011 Reserved 100 Reserved 101 No data 110 Implicit Write-back 111 Normal Data
HTRDY#	O 0.9~1.75V – M	Target Ready: During write cycles, response agent will drive TRDY# to indicate it is ready to accept data.
DRDY#	I/O 0.9~1.75V – M	Data Ready: DRDY# is driven by the bus owner whenever the data is valid on the bus.
DBSY#	I/O 0.9~1.75V – M	Data Bus Busy: Whenever the data is not valid on the bus with DRDY# is deserted, DBSY# deasserted to hold the bus.
HDSTBP[3:0]#	I/O 0.9~1.75V – M	Source synchronous data strobe used to latch data at falling edge HD[15:0], DBI0# are latched by HDSTBP0# HD[31:16], DBI1# are latched by HDSTBP1# HD[47:32], DBI2# are latched by HDSTBP2# HD[63:48], DBI3# are latched by HDSTBP3#
HD[63:0]#	I/O 0.9~1.75V – M	Host Data Bus

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Host Bus Interface(3)

Pin Name	Pin Attr	Description
HDSTBN[3:0]#	I/O 0.9~1.75V–M	Source synchronous data strobe used to latch data at falling edge HD[15:0], DBI0# are latched by HDSTBN0# HD[31:16], DBI1# are latched by HDSTBN1# HD[47:32], DBI2# are latched by HDSTBN2# HD[63:48], DBI3# are latched by HDSTBN3#
HNCOMP	I M	GTL N-MOS Compensation Input
HPCOMP	I M	GTL P-MOS Compensation Input
HVREF[4:0]	I M	AGTL+ I/O reference voltage
HNCOMPVREF		Reserved

DRAM Controller(1)

Pin Name	Pin Attr	Description
SDRCLKI		Reserved
FWDSDCLKO	O 2.5V - M	SDRAM Forward Clock Output
MA[14:0]	O 2.5V - M	System Memory Address Bus
SRAS#	O 2.5V - M	SDRAM Row Address Strobe
SCAS#	O 2.5V - M	SDRAM Column Address Strobe
SWE#	O 2.5V - M	SDRAM Write Enable
CS[5:0]#	O 2.5V - M	DRAM Chip Select
DQM[7:0]#	O 2.5V - M	SDRAM Input/Output Data Mask
DQS[7:0]	I/O 2.5V - M	DDR Data Strobe
MD[63:0]	I/O 2.5V - M	System Memory Data Bus
CKE[5:0]	O 2.5V - AUX	SDRAM Clock Enable

DRAM Controller(2)

Pin Name	Pin Attr	Description
S3AUXSW# (CKE6)	O (open-drain) 2.5V - AUX	Aux power switch for ACPI-S3 state, low active.
DDRVREF[A:B]	I M	DDR I/O Reference Voltage
DDRCOMP_P	I M	P-MOS Compensation Input
DDRCOMP_N	I M	N-MOS Compensation Input

MuTIOL 1G Interface

Pin Name	Pin Attr	Description
ZCLK	I 3.3V - M	SiS MuTIOL 1G clock
ZUREQ/ZDREQ	I/O 1.8V - M	SiS MuTIOL 1G Control pins
ZSTB[1:0]	I/O 1.8V - M	SiS MuTIOL 1G Strobe
ZSTB[1:0]#	I/O 1.8V - M	Strobe Compliment
ZAD[16:0]	I/O 1.8V - M	Address/Data/DBI Pins
ZVREF	I M	SiS MuTIOL 1G Reference Voltage
ZCMP_N	I M	N-MOS Compensation Input
ZCMP_P	I M	P-MOS Compensation Input

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AGP Interface

Pin Name	Pin Attr	Description
AGPCLK	I 3.3V – M	AGP Clock
AFRAME#	I/O 1.5V - M	AGP Frame#
AIRDY#	I/O 1.5V - M	AGP Initiator Ready
ATRDY#	I/O 1.5V - M	AGP Target Ready
ASTOP#	I/O 1.5V - M	AGP Stop#
ADEVSEL#	I/O 1.5V - M	AGP Device Select
ASERR#	I 1.5V - M	AGP System Error

AGP Interface(1)

Pin Name	Pin Attr	Description
AGPCOMP_N	I M	N-MOS Compensation Input
RBF#	I 1.5V - M	Read Buffer Full
WBF#	I 1.5V - M	Write Buffer Full
AD_STB[1:0]	I/O 1.5V - M	AD Bus Strobe
AD_STB[1:0]#	I/O 1.5V - M	AD Bus Strobe Compliment
SB_STB	I 1.5V - M	Side Band Strobe
SB_STB#	I 1.5V - M	Side Band Strobe Compliment
GC_DET#	I 1.5V - M	AGP v3.0 strap
AGPVREF	I M	AGP Reference Voltage
AGPCOMP_P	I M	P-MOS Compensation Input

AGP Interface(2)

Pin Name	Pin Attr	Description
AREQ#	I 1.5V - M	AGP Bus Request
AGNT#	O 1.5V - M	AGP Bus Grant
ADBI_LO	I/O 1.5V - M	DBI of AAD[15:0]
AAD[31:0]	I/O 1.5V - M	AGP Address/Data Bus
AC/BE[3:0]	I/O 1.5V - M	AGP Command/Byte Enable
APAR	I/O 1.5V - M	AGP Parity
ST[2:0]	O 1.5V - M	AGP Status Bus
PIPE#	I 1.5V - M	AGP Pipeline Request in v2.0 DBI of AAD[31:16] in v3.0
SBA[7:0]	I/O 1.5V - M	Side Band Address

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Test Mode / Hardware Trap / Power Management

Pin Name	Pin Attr	Description
DLLEN#	I/O 3.3V/5V – M	Hardware Trap pin (refer to section 5)
TRAP[1:0]	I 3.3V/5V – M	Hardware Trap pins (refer to section 5)
ENTEST	I 3.3V/5V – M	Test Mode enable pin
TESTMODE[2:0]	I 3.3V/5V – M	Test Mode select pin Nand Tree Test: 100
AUXOK	I 3.3V – AUXI	Auxiliary Power OK : This signal is supplied from the power source of resume well. It is also used to reset the logic in resume power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
PCIRST#	I 3.3V – AUXI	PCI Bus Reset : PCIRST# is supplied from SiS®963L HyperZip Media IO.
PWROK	I 3.3V – AUXI	Main Power OK : A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, CPURST and PCIRST# will all be asserted until after PWROK goes high for 24 ms.

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Host Bus Interface

Name	Pin Attr	Description
FERR#	I 0.8V/2.65V -M	**Floating Point Error:** CPU will assert this signal upon a floating point error occurring.
IGNNE#	OD 0.8V/2.65V -M	**Ignore Numeric Error:** IGNNE# is asserted to inform CPU to ignore a numeric error.
NMI	OD 0.8V/2.65V -M	**Non-Maskable Interrupt:** A rising edge on NMI will trigger a non-maskable interrupt to CPU.
INTR	OD 0.8V/2.65V -M	**Interrupt Request:** High-level voltage of this signal conveys to CPU that there is outstanding interrupt(s) needed to be serviced.
APICD1 / **GPIOFF#** **APICD0 /** **THERM2#**	I/OD I I/OD I 0.8V/2.65V -M	**APIC Data: APICD[1:0]** These two signals are used to send and receive APIC data. **GPIO OFF:** Turn off the system when input a low level signal. **Thermal 2:** Assert a SMI#/SCI# when input a low level signal.
CPUSLP#	OD 0.8V/2.65V -M	**CPU Sleep:** The CPUSLP# can be used to force CPU enter the Sleep state.
STPCLK#	OD 0.8V/2.65V -M	**Stop Clock:** STPCLK# will be asserted to inhibit or throttle CPU activities upon a pre-defined power management event occurs.
SMI#	OD 0.8V/2.65V -M	**System Management Interrupt:** SMI# will be asserted when a pre-defined power management event occurs.
INIT#	OD 0.8V/2.65V -M	**Initialization:** INIT is used to re-start the CPU without flushing its internal caches and registers. In Pentium III platform it is active high. This signal requires an external pull-up resistor tied to VTT.
APICCK/ **LDTREQ# /** **AGPBUSY#**	I 2.5V/3.3V -M	**APIC Clock:** This signal is used to determine when valid data is being sent over the APCI bus. **LDTREQ# / AGPBUSY# (New function in SiS963 B stepping and LDTREQ# for K8 use only)** When a low active signal inputs, it will wake up system from C3/S1.
A20M#	OD 0.8V/2.65V - M	**Address 20 Mask:** When A20M# is asserted, the CPU A20 signal will be forced to “0”

MuTIOL 1G Connect Interface

Name	Pin Attr	Description
ZCLK	I 3.3V - M	MuTIOL 1G I/O Connect Clock
ZUREQ	I/O 1.8V - M	MuTIOL 1G I/O Conect Controll pins
ZDREQ	I/O 1.8V - M	MuTIOL 1G I/O Conect Controll pins
ZSTB[1:0]	I/O 1.8V - M	MuTIOL 1G I/O Connect Strobe
ZSTB[1:0]#	I/O 1.8V - M	MuTIOL 1G Strobe Compliment
ZAD[16:0]	I/O 1.8V - M	MuTIOL 1G Address/Data pins
ZVREF	I -M	MuTIOL 1G I/O reference voltage
ZCMP_N	I -M	MuTIOL 1G N-MOS Compensation Input
ZCMP_P	I -M	MuTIOL 1G P-MOS Compensation input

PCI Interface(1)

Name	Pin Attr	Description
PCICLK	I 3.3V/5V -M	**PCI Clock:** The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS963. It runs at the same frequency and skew of the PCI local bus.
C/BE[3:0]#	I/O 3.3V/5V -M	**PCI Bus Command and Byte Enables:** PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS963 is a PCI bus master and inputs when it is a PCI slave.
INT[A:D]#	I 3.3V/5V – M	**PCI interrupt A,B,C,D:** The PCI interrupts will be connected to the inputs of the internal Interrupt controller through the rerouting logic associated with each PCI interrupt.
PLOCK#	I/O 3.3V/5V -M	**PCI Lock:** When PLOCK# is sampled asserted at the beginning of a PCI cycle, SiS963 considers itself being locked and remains in the locked state until PLOCK# is sampled and negated at the following PCI cycle.

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PCI Interface(2)

Name	Pin Attr	Description
IRDY#	I/O 3.3V/5V -M	**Initiator Ready:** IRDY# is an output when the SiS963 is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS963 is a PCI slave, IRDY# is an input pin.
TRDY#	I/O 3.3V/5V -M	**Target Ready:** TRDY# is an output when the SiS963 is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS963 is a PCI master, it is an input pin.
STOP#	I/O 3.3V/5V -M	**Stop#:** STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnection, retry, and target-abortion sequences on the PCI bus.
DEVSEL#	I/O 3.3V/5V -M	**Device Select:** As a PCI target, SiS963 asserts DEVSEL# by doing positive or subtractive decoding. SiS963 positively asserts DEVSEL# when the DRAM address is being accessed by a PCI master, PCI configuration registers or embedded controllers' registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M memory space are responded subtractively. The DEVESEL# is an input pin when SiS963 is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
PAR	I/O 3.3V/5V -M	**Parity:** SiS963 drives out Even Parity covering AD[31:0] and C/BE[3:0]#. It does not check the input parity signal.
FRAME#	I/O 3.3V/5V -M	**Frame#:** FRAME# is an output when the SiS963 is a PCI bus master. The SiS963 drives FRAME# to indicate the beginning and duration of an access. When the SiS963 is a PCI slave device, FRAME# is an input signal.
PREQ[4:0]#	I 3.3V/5V -M	**PCI Bus Request:** PCI Bus Master Request Signals

PCI Interface(3)

Name	Pin Attr	Description
PGNT[4:0]#	O 3.3V –M	**PCI Bus Grant:** PCI Bus Master Grant Signals
PREQ5# / GPIO5	I I/O 3.3V/5V-M	**PCI Bus Request:** PCI Bus Master Request Signal
PGNT5# / GPIO6	O I/O 3.3V- M	**PCI Bus Grant:** PCI Bus Master Grant Signal
PCIRST#	O 3.3V –M	**PCI Bus Reset:** PCIRST# will be asserted during the period when PWROK is low, and will be kept on asserting until about 24ms after PWROK goes high.
SERR#	I 3.3V/5V –M	**System Error:** When sampled active low, a non-maskable interrupt (NMI) can be generated to CPU if enabled.
AD[31:0]	I/O 3.3V/5V -M	**PCI Address /Data Bus:** In address phase: 1.When the SiS963 is a PCI bus master, AD[31:0] are output signals. 2.When the SiS963 is a PCI target, AD[31:0] are input signals. In data phase: 1.When the SiS963 is a target of a memory read/write cycle, AD[31:0] are floating. 2.When the SiS963 is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.

IDE Interface(1)

Name	Pin Attr	Description
IDA[15:0]	I/O 3.3V/5V -M	Primary Channel Data Bus
IDB[15:0]	I/O 3.3V/5V -M	Secondary Channel Data Bus
IDECSA[1:0]#	O 3.3V -M	Primary Channel CS[1:0]

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IDE Interface(2)

Name	Pin Attr	Description
IDECSB[1:0]#	O 3.3V -M	Secondary Channel CS[1:0]
IIOR[A:B]#	O 3.3V -M	Primary/Secondary Channel IOR# Signals
IIOW[A:B]#	O 3.3V -M	Primary/Secondary Channel IOW# Signals
ICHRDY[A:B]	I 3.3V/5V -M	Primary/Secondary Channel ICHRDY# Signals
IDREQ[A:B]	I 3.3V/5V -M	Primary/Secondary Channel DMA Request Signals
IDACK[A:B]#	O 3.3V -M	Primary/Secondary Channel DMACK# Signals
IIRQ[A:B]	I 3.3V/5V -M	Primary/Secondary Channel Interrupt Signals
IDSAA[2:0]	O 3.3V -M	Primary Channel Address [2:0]
IDSAB[2:0]	O 3.3V -M	Secondary Channel Address [2:0]
CBLID[A:B]	I 3.3V/5V -M	Primary/Secondary Ultra-66 Cable ID

Power Management Interface(1)

Name	Pin Attr	Description
ACPILED	OD <=5V -AUX	**ACPILED :** ACPILED can be used to control the blinking of an LED at the frequency of 1 Hz to indicate the system is at power saving mode.
EXTSMI# **(GPIO3)**	I I/O 3.3V/5V -M	**External SMI#:** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI# event to the ACPI compatible power management unit.
PME#	I 3.3V/5V -AUX	**PME# :** When the system is in power-down mode, an active low event on PME# will cause the PSON# to go low and hence turn on the power supply. When the system is in suspend mode, an active PME# event will cause the system wakeup and generate an SCI/SMI#.

Power Management Interface(2)

Name	Pin Attr	Description
PSON#	OD <=5V -AUX	**ATX Power ON/OFF control:** PSON# is used to control the on/off state of the ATX power supply. When the ATX power supply is in the OFF state, an activated power-on event will force the power supply to ON state.
AUXOK	I 3.3V -AUX	**Auxiliary Power OK:** This signal is supplied from the AUX power source. It is also used to reset the logic in AUX power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
PWRBTN#	I 3.3V/5V -AUX	**Power Button:** This signal is from the power button switch and will be monitored by the ACPI-compatible power management unit to switch the system between working and sleeping states.
THERM# **(GPIO2)**	I 3.3V/5V -M	**Thermal Alarm:** When a low active signal inputs, it will assert a SMI#/SCI# event and assert CPU throttling.
EXTSMI# **(GPIO3)**	I 3.3V/5V -M	**External SMI#:** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI# event to the ACPI compatible power management unit.
CLKRUN# **(GPIO4)**	I/O 3.3V/5V – M	**Clock Run: (for Mobile only)** Used by PCI and LPC peripherals to request the system PCI clock to re-start, or prevent PCI clock stopping. An external pull-up to the MAIN power is required.
GPWAK# **(GPIO7)**	I 3.3V/5V -AUX	**General Purpose Wake-Up Signal:** Used to wake up the system from S1/S3/S4/S5.
RING **(GPIO8)**	I 3.3V/5V -AUX	**Ring Indication:** An active RING pulse and lasting for more than 4ms will cause a wakeup event for system to wake from S1~S5.
AC_SDIN2, 3 **(GPIO9, 10)**	I 3.3V/5V -AUX	**AUDIO Wake-Up Signal:** Used to wake up the system from S1/S3/S4/S5.
STP_PCI# / **AGPSTOP#** **(GPIO11)**	O OD 3.3V/5V – AUX	**Stop PCI Clock: (for Mobile only)** Used to stop the system PCI clock. Used to support PCI CLKRUN# protocol. **AGP Clock Stop: (for Mobile only, if GPIO14 is used to be S3AUXSW#,** **new MUX function in SiS963 B stepping)** AGPSTOP# is used to stop the AGP_CLOCK output from clock generator during C3/S1 state.

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Power Management Interface(3)

Name	Pin Attr	Description
DPRSLPVR (GPIO13)	O 3.3V/5V -AUX	**Deeper Sleep (for Mobile only):** Used to lower the voltage of VRM during CPU entered the deeper power saving mode. Because this signal will be at input mode after the Clear RTC operation, an external pulled down resistor is required for this signal. When this signal is high, the voltage regulator outputs the Deeper Sleep voltage. When this signal is low (default), the voltage regulator output the Normal voltage. DPRSLP# can be used to lower the Intel processor voltage during C3/S1 state.
AGPSTOP# / S3AUXSW# (GPIO14)	OD 3.3V/5V -AUX	**AGP Clock Stop (for Mobile only):** AGPSTOP# is used to stop the AGP_CLOCK output from clock generator during C3/S1 state. **S3AUXSW#:(for SiS755 and SiSR658 use only, new function in SiS963 B stepping)** The signal will keep low in S3 state.
VR_HILO# (GPIO15)	O 3.3V/5V -AUX	**Voltage Regulator HI / LO (for Mobile only):** This ping is used to select an appropriate VID for voltage regulator. A low level indicates the Battery Optimal mode. A high level indicates the Maximum Performance mode.
LO_HI# (GPIO16)	OD 1.5V/5V -AUX	**LO_HI# (for Mobile only):** This pin is connected to the processor. A high level indicates the Battery Optimal mode. A low level indicates the Maximum Performance mode.
VGATEM# (GPIO17)	OD 1.5V/5V -AUX	**VGATEM# (for Mobile only):** Output pin, it is used to mask the PWRGOOD of processor core voltage regulator.
RTC32KHZ (GPIO18)	O 3.3V/5V -AUX	**RTC32KHz output: (Mobile only)** Support RTC32KHz clock output in S0~S5.
THERM2# (APICD0)	I 0.8V/2.65V -M	**Thermal Alarm2: (GTL level)** When a low active signal inputs, it will assert a SMI#/SCI# event.
GPIOFF# (APICD1)	I 0.8V/2.65V -M	**GPIO OFF: (GTL level)** When a low level signal inputs, it will turn off the system. Then, the system can only be woken up again by PWRBTN#.
CPUSTP# (GPIO12)	OD 1.5V/5V -AUX	**CPU Clock Stop (for Mobile only):** For Intel Mobile processor, this signal can be used to stop the clock to the processor. This signal connected to the DPSLP# signal of Pentium 4 processor that can let the processor enter the Deep Sleep state as well (recommended). For AMD processor, this signal can be to reduce processor voltage during C3/S1 state.

Keyboard Controller Interface

Name	Pin Attr	Description
KBDAT (GPIO15)	I/OD 3.3V/5V -AUX	**Keyboard Dada:** When the internal keyboard controller is enabled, this pin is used as the keyboard data signal.
KBCLK (GPIO16)	I/OD 3.3V/5V -AUX	**Keyboard Clock:** When the internal keyboard controller is enabled, this pin is used as the keyboard clock signal.
PMDAT (GPIO17)	I/OD 3.3V/5V -AUX	**PS2 Mouse Data:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as PS2 mouse data signal.
PMCLK (GPIO18)	I/OD 3.3V/5V -AUX	**PS2 Mouse Clock:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as the PS2 mouse clock signal.

LPC Interface

Name	Pin Attr	Description
LAD[3:0]	I/O 3.3V/5V-M	**LPC Address/Data Bus:** LPC controller drives these four pins to transmit LPC command, address, and data to LPC device.
LDRQ#	I 3.3V/5V-M	**LPC DMA Request 0:** This pin is used by LPC device to request DMA cycle.
LDRQ1# (GPIO1)	I 3.3V/5V-M	**LPC DMA Request 1:** This pin is used by LPC device to request DMA cycle.
LFRAME#	O 3.3V -M	**LPC Frame:** This pin is used to notify LPC device that a start or a abort LPC cycle will occur.
SIRQ	I/O 3.3V/5V -M	**Serial IRQ:** This signal is used as the serial IRQ line signal.

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RTC Interface

Name	Pin Attr	Description
BATOK	I 3.3V -RTC	**Battery Power OK:** When the internal RTC is enabled, this signal is used to indicate that the power of RTC well is stable. It is also used to reset the logic in RTC well. If the internal RTC is disabled, this pin should be tied low.
OSC32KHI	I 3.3V-RTC	**RTC 32.768 KHz Input:** When internal RTC is enabled, this pin provides the 32.768 KHz clock signal from external crystal or oscillator.
OSC32KHO	O 3.3V -RTC	**RTC 32.768 KHz Output:** When internal RTC is enabled, this pin should be connected with the other end of the 32.768 KHz crystal or left unconnected if an external oscillator is used.
PWROK	I 3.3V-RTC	**Main Power OK**: A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, PCIRST# will all be asserted until after PWROK goes high for 12 ms.

AC'97 Interface

Name	Pin Attr	Description
AC_BIT_CLK	I 3.3V/5V -M	**AC'97 Bit Clock:** This signal is a 12.288MHz serial data clock, which is generated by primary Codec.
AC_RESET#	O 3.3V -AUX	**AC'97 Reset:** Hardware reset signal for external Codecs.
AC_SDIN0	I 3.3V/5V -AUX	**AC'97 Serial Data Input :** Serial data input from primary Codec.
AC_SDIN1	I 3.3V/5V -AUX	**AC'97 Serial Data Input:** Serial data input from secondary Codec. When Modem Codec is used, this pin dedicate to Modem Serial data input.
AC_SDIN[3:2] (GPIO[10:9])	I 3.3V/5V -AUX	**AC'97 Serial Data Input:** Serial data input from third and forth Audio Codec.
AC_SDOUT	O 3.3V -M	**AC'97 Serial Data Output:** Serial data output to Codecs.
AC_SYNC	O 3.3V -M	**AC'97 Synchronization:** This is a 48KHz signal, which is used to synchronize the Codecs.

General Purpose I/O

Name	Pin Attr	Description
GPIO[6:0]	I/O 3.3V/5V -M	**GPIO:** Can be a General Purpose Input or Output.
GPIO[15:7]	I/O 3.3V/5V -AUX	**GPIO:** Can be a General Purpose Input or Output.
GPIO[18:16]	O 3.3V/5V – AUX	**GPO:** Can be a General Purpose Output.
GPIO[20:19]	OD 3.3V/5V – AUX	**GPIO:** Can be a General Purpose Input or Output.
GPIO[24:21]	I 3.3V/5V -AUX	**GPI:** Can be a General Purpose Input.

Hardware Trap Signals

Name	Pin Attr	Description
IPB_OUT0	O 3.3V -AUX	**IPB_OUTO:** Hardware Trap to select MuTIOL 1G clock PLL enable/disable.
IPB_OUT1	O 3.3V -AUX	**IPB_OUT1:** Hardware Trap to select MuTIOL 1G operation mode.

Legacy I/O and Miscellaneous Signals

Name	Pin Attr	Description
SPK	O 3.3V -M	**Speaker output:** The SPK is connected to the system speaker.
ENTEST	I 3.3V/5V -M	SiS963 Test Mode Enable Pin
OSCI	I 3.3V -M	14.318 MHz. Clock In

5.3 SiS963 South Bridge

MAC Interface(1)

Name	Pin Attr	Description
RXER	I 3.3V/5V -AUX	**RX Packet Error:** This event is signaled after the last received descriptor in a failed packet reception that has been updated with valid status.
OSC25MHI	I 3.3V/5V -AUX	**PHY 25MHz Clock Input:** This pin provides the 25MHz clock signal input form external crystal or oscillator.
OSC25MHO	O 3.3V/5V -AUX	**PHY 25Mhz Clock Output:** This pin should be connected with the other end of the 25Mhz crystal or left unconnected if an external oscillator is used.
MDC	O 3.3V -AUX	**Management Data Clock:** Clock signal with a maximum rate of 2.5MHz used to transfer management data for the external physical unit on the MIIMDIO pin.
TXD[0:3]	O 3.3V -AUX	**Transmit Data:** This is a group of 4 data signals which are driven synchronous to the TXCLK for transmission to the external physical unit.
RXD[0:3]	I 3.3V/5V -AUX	**Receive Data:** This is a group of 4 data signals aligned on nibble boundaries which are driven synchronous to the RXCLK by the external physical unit.
TXEN	O 3.3V -AUX	**Transmit Enable:** When set to a 1, and the transmit state machine is idle, then the transmit state machine becomes active. This bit will read back as a 1 whenever the transmit state machine is active. After initial power-up, software must insure that the transmitter has completely reset before setting this bit.
MDIO	I/O 3.3V/5V -AUX	**Management Data I/O:** Bi-direction signal used to transfer management information for the external physical unit. Requires external pull-up resistor.
EEDO (GPIO23)	I 3.3V -AUX	**Serial EEPROM Data Output:** During serial EEPROM access cycle, SiS963 will read the contents of the EEPROM serially through this pin.
EECS (GPIO24)	O 3.3V -AUX	**Serial EEPROM Chip Select:** This pin enables the EEPROM during loading of the Ethernet configuration data.
EESK (GPIO21)	O 3.3V -AUX	**Serial EEPROM Clock:** This pin provides the clock for the serial EEPROM.
RXDV	I 3.3V/5V -AUX	**Receive Data Vali**d: This indicates that the external physical unit is presenting recovered and decoded nibbles on the RXD[3:0] and that RXCLK is synchronous to the recovered data. This signal will encompass the frame, starting with the Start-Of-Frame delimiter and excluding the End-Of-Frame delimiter.

MAC Interface(2)

Name	Pin Attr	Description
COL	I 3.3V/5V -AUX	**Collision Detect:** This signal is asserted high asynchronous by the external physical unit upon detection of a collision on the medium. It'll remain asserted as long as the collision condition persists.
CRS	I 3.3V/5V -AUX	**Carrier Sense:** This signal is asserted high asynchronously by the physical unit upon detection of a non-idle medium.
RXCLK	I 3.3V/5V -AUX	**Receive Clock:** A continuous clock that is recovered from the incoming data. During 100Mb/s operation RXCLK is 25MHz and during 10Mb/s this is 2.5MHz.
TXCLK	I 3.3V/5V -AUX	**Transmit Clock:** A continuous clock that is sourced by the physical unit. During 100Mb/s operation RXCLK is 25MHz and during 10Mb/s this is 2.5MHz.
CLK25M (GPIO11)	I 3.3V/5V -AUX	**External 25MHz Clock Input:** This pin provides direct 25Mhz OSC Clock in to MAC controller.
EEDI (GPIO22)	O 3.3V/5V -AUX	**Serial EEPROM Data Input:** During serial EEPROM access cycle, SiS963 will use this pin to serially write OP codes, addresses and data into the serial EEPROM.

1394 Interface

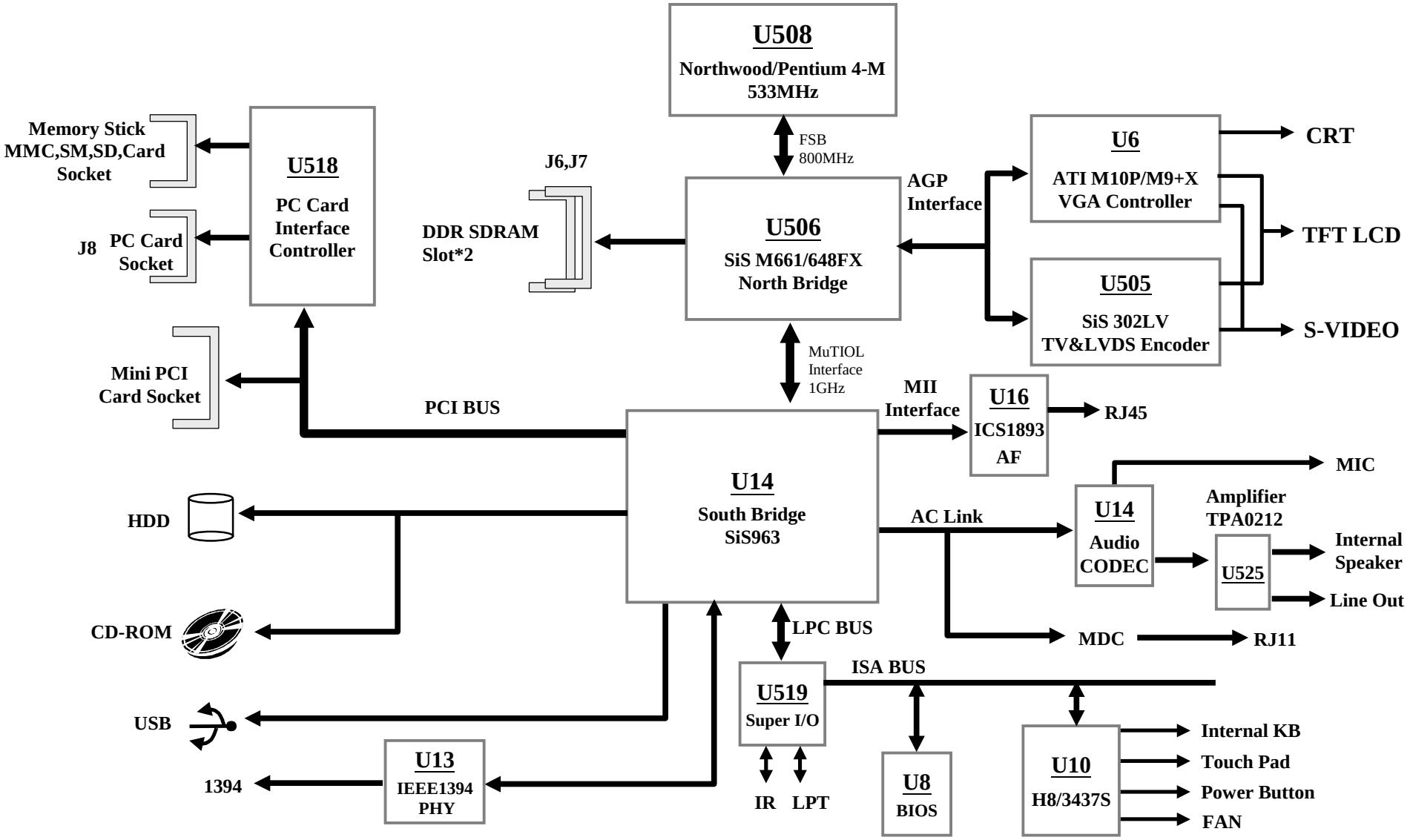
Name	Pin Attr	Description
LINKON	I 3.3V -AUX	**Link-on event input:** Occurrence of a link-on event from PHY.
LREQ	O 3.3V –AUX	**Link Request:** This pin drives a link request from SiS963 to PHY.
LPS	O 3.3V –AUX	**Link Power Status:** This pin indicates that the link is powered and functional.
D[7:0]	I/O 3.3V –AUX	**Link Data[7:0]:** Bi-directional 8-bit link data bus.
CTL[1:0]	I/O 3.3V –AUX	**Link Data[7:0]:** Bi-directional 2-bit link control.
SCLK	I 3.3V –AUX	**Link Clock input:** 12.288, 24.576 or 49.152MHz clock (synchronized to the PHY transmit clock).

5.3 SiS963 South Bridge

USB Interface

Name	Pin Attr	Description
OSC12MHI	I 3.3V/5V -AUX	**UTMI 12MHz Clock Input:** This pin provides the 12MHz clock signal input form external crystal or oscillator.
OSC12MHO	O 3.3V/5V -AUX	**UTMI 12Mhz Clock Output:** This pin should be connected with the other end of the 12Mhz crystal or left unconnected if an external oscillator is used
USBCLK48M	I 3.3V/5V -M	**USB 48 MHz clock input:** This signal provides the fundamental clock for the USB Controller.
OC[0:5]#	I/O 3.3V/5V - AUX	**USB Port 0-5 Overcurrent Detection:** OC[0:5]# are used to detect the overcurrent condition of USB Ports 0-5.
UV[3,0]+, **UV[3,0]-**	I/O 3.3V - AUX	**USB Port [3:**0] **Differentia**l: These differential pairs are used to transmit Data/Address /Command signals for ports 3 and 0. (USB controller 0).
UV[4,1]+, **UV[4,1]-**	I/O 3.3V - AUX	**USB Port [4:1] Differentia**l: These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 1. (USB controller 1).
UV[5,2]+, **UV[5,2]-**	I/O 3.3V - AUX	**USB Port [5,2] Differentia**l: These differential pairs are used to transmit Data/Address/Command signals for ports 5 and 2. (USB controller 2).
USBREF	I 3.3V – AUX	**USB reference resistor inpu**t: A resistor should be connected to USBVSS from this pin for IO impedance calibration.

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

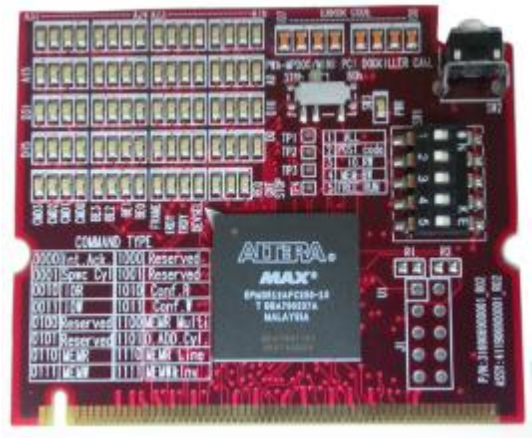
Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to the port by the debug card plug at MINI PCI slot.

7. Maintenance Diagnostics

7.1.1 Diagnostic Tool for Mini PCI Slot :

The Mini PCI DOGkiller card is a single-step debug tool which utilizes Mini PCI interface (Type III A) and is able to hold a PCI bus cycle so that address, data and control bus states on PCI bus can be inspected. Especially, the tool can help an engineer trace address/data bus for BIOS read cycles as soon as power on and debug open or short circuit problems easily. Usually, this sort of problem will make a PC motherboard fail to boot.



P/N:411906900001
Description: PWA; PWA-MPDOG/MINI PCI DOGKILLER CARD
Note: Order it from MIC/TSSC

7.2 Error Codes - 1

Following is a list of error codes in sequent display on the debug board.

POST (HEX)	DESCRIPTION
10H	Some Type Of Long Reset
11H	Turn off FASTA20 for POST
12H	Signal Power On Reset
13H	Initialize the Chipset
14H	Search For ISA Bus VGA Adapter
15H	Reset Counter/Timer 1
16H	user register configure through CMOS
17H	Size Memory
18H	Dispatch To RAM Test
19H	checksum the ROM
1AH	Reset PIC's
1BH	Initialize Video Adapter(s)
1CH	Initialize Video (6845 Regs)
1DH	Initialize Color Adapter
1EH	Initialize Monochrome Adapter
1FH	Test 8237A Page Registers
20H	Test Keyboard
21H	Test Keyboard Controller
22H	Check If CMOS Ram Valid
23H	Test Battery Fail & CMOS X-SUM
24H	Test the DMA controllers
25H	Initialize 8237A Controller
26H	Initialize Int Vectors

POST (HEX)	DESCRIPTION
27H	RAM Quick Sizing
28H	Protected mode entered safely
29H	RAM test completed
2AH	Protected mode exit successful
2BH	Setup Shadow
2CH	Going To Initialize Video
2DH	Search For Monochrome Adapter
2EH	Search For Color Adapter
2FH	Signon messages displayed
30H	special init of keyboard ctrl
31H	Test If Keyboard Present
32H	Test Keyboard Interrupt
33H	Test Keyboard Command Byte
34H	TEST, Blank and count all RAM
35H	Protected mode entered safely (2).
36H	RAM test complete
37H	Protected mode exit successful
38H	Update OUTPUT port
39H	Setup Cache Controller
3AH	Test If 18.2Hz Periodic Working
3BH	test for RTC ticking
3CH	initialize the hardware vectors
3DH	Search and Init the Mouse

7.2 Error Codes - 2

Following is a list of error codes in sequent display on the debug board.

POST (HEX)	DESCRIPTION
3EH	Update NUMLOCK status
3FH	special init of COMM and LPT ports
40H	Configure the COMM and LPT ports
41H	Initialize the floppies
42H	Initialize the hard disk
43H	Initialize option ROMs
44H	OEM's init of power management
45H	Update NUMLOCK status
46H	Test For Coprocessor Installed
47H	OEM functions before boot
48H	Dispatch To Op. Sys. Boot
49H	Jump Into Bootstrap Code

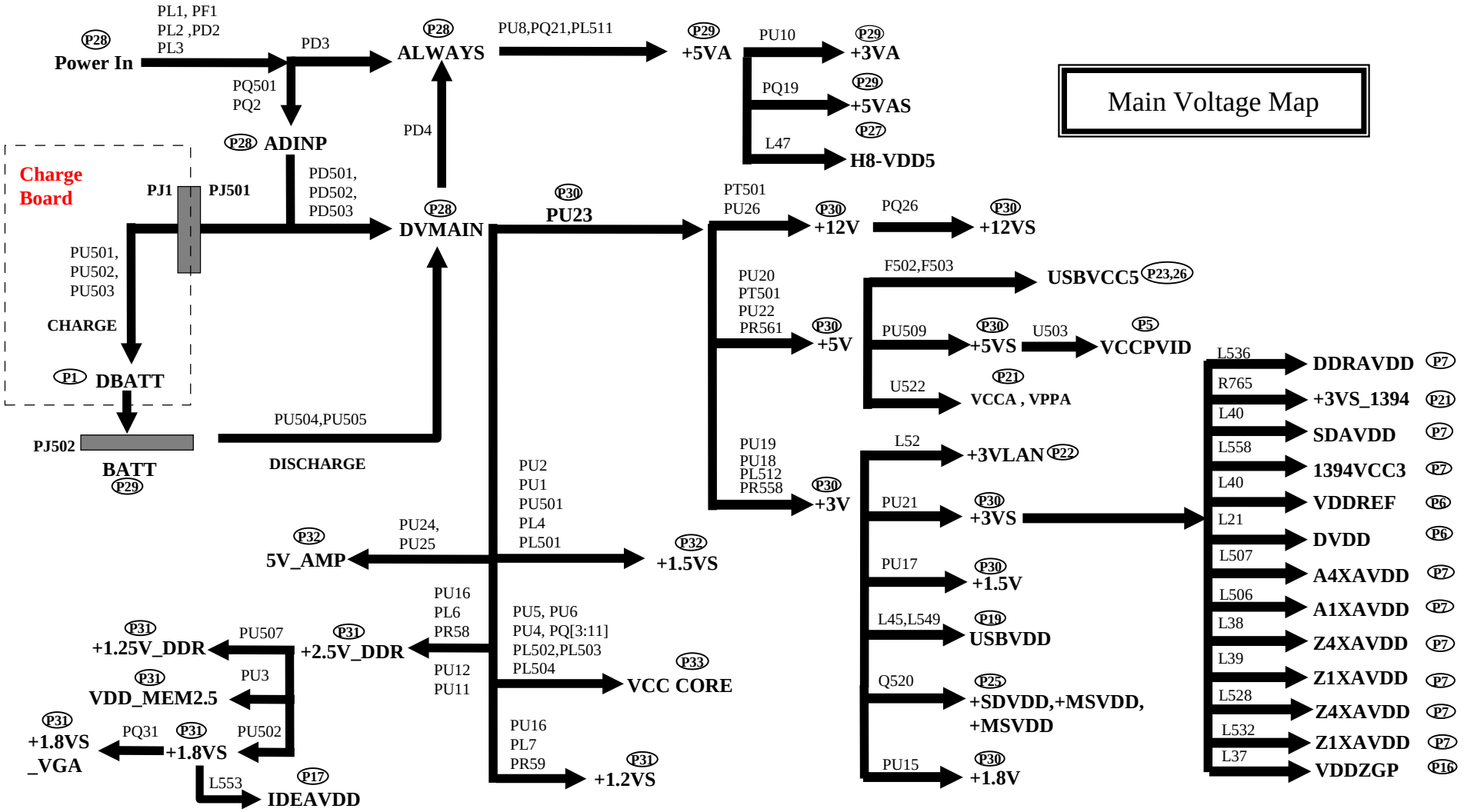
8. Trouble Shooting

- 8.1 No Power
- 8.2 Battery Can not Be Charged
- 8.3 No Display
- 8.4 LCD No Display or Picture Abnormal
- 8.5 External Monitor No Display or Color Abnormal
- 8.6 Memory Test Error
- 8.7 Keyboard and Touch Pad Test Error
- 8.8 Hard Disk Drive Test Error
- 8.9 CD-ROM Drive Test Error
- 8.10 USB Port Test Error
- 8.11 PC Card Socket Test Error
- 8.12 LAN Test Error
- 8.13 Audio Failure
- 8.14 Mini PCI Test Error

8555 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens ,power indicator does not light up.



8555 N/B Maintenance

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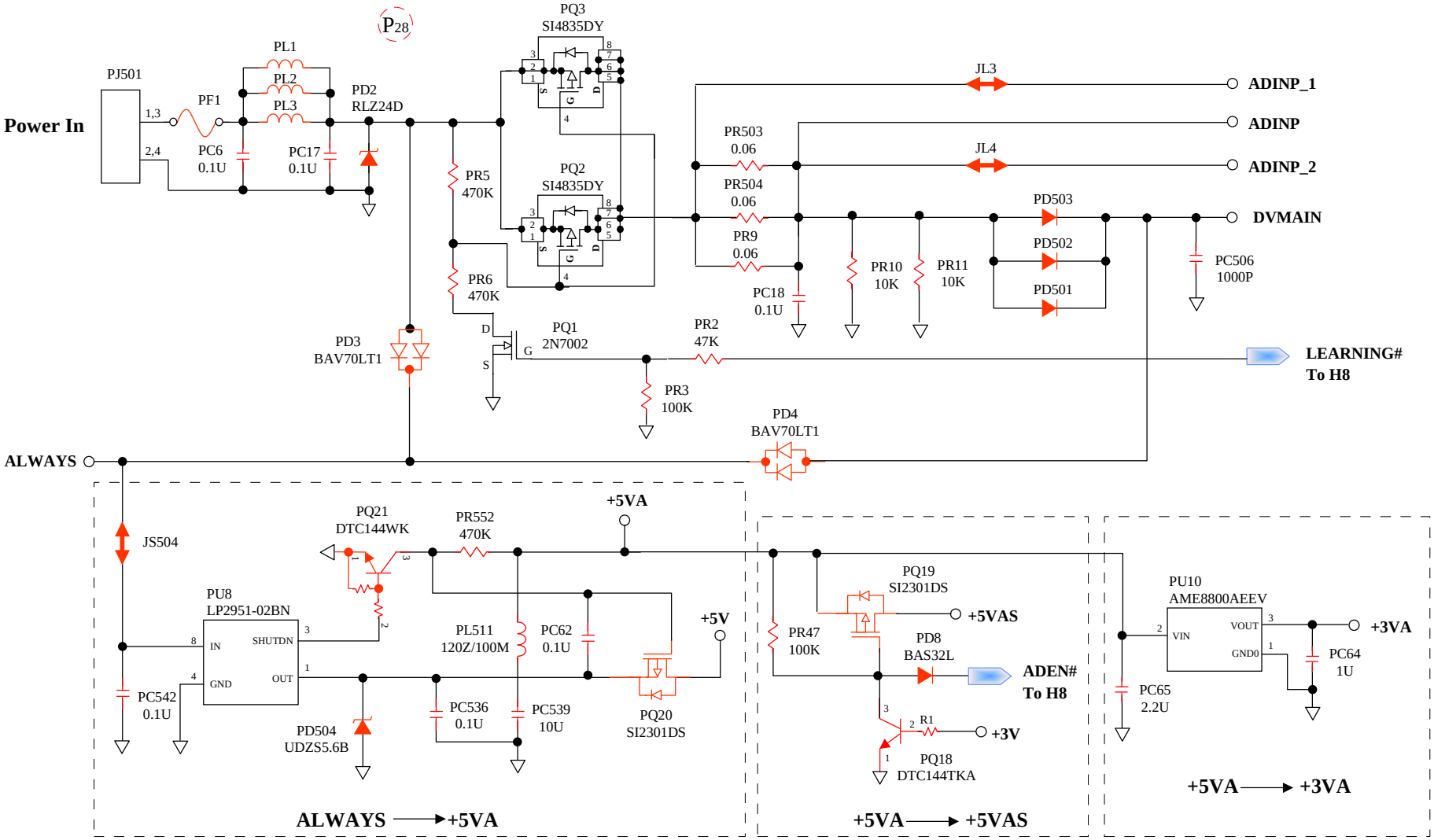
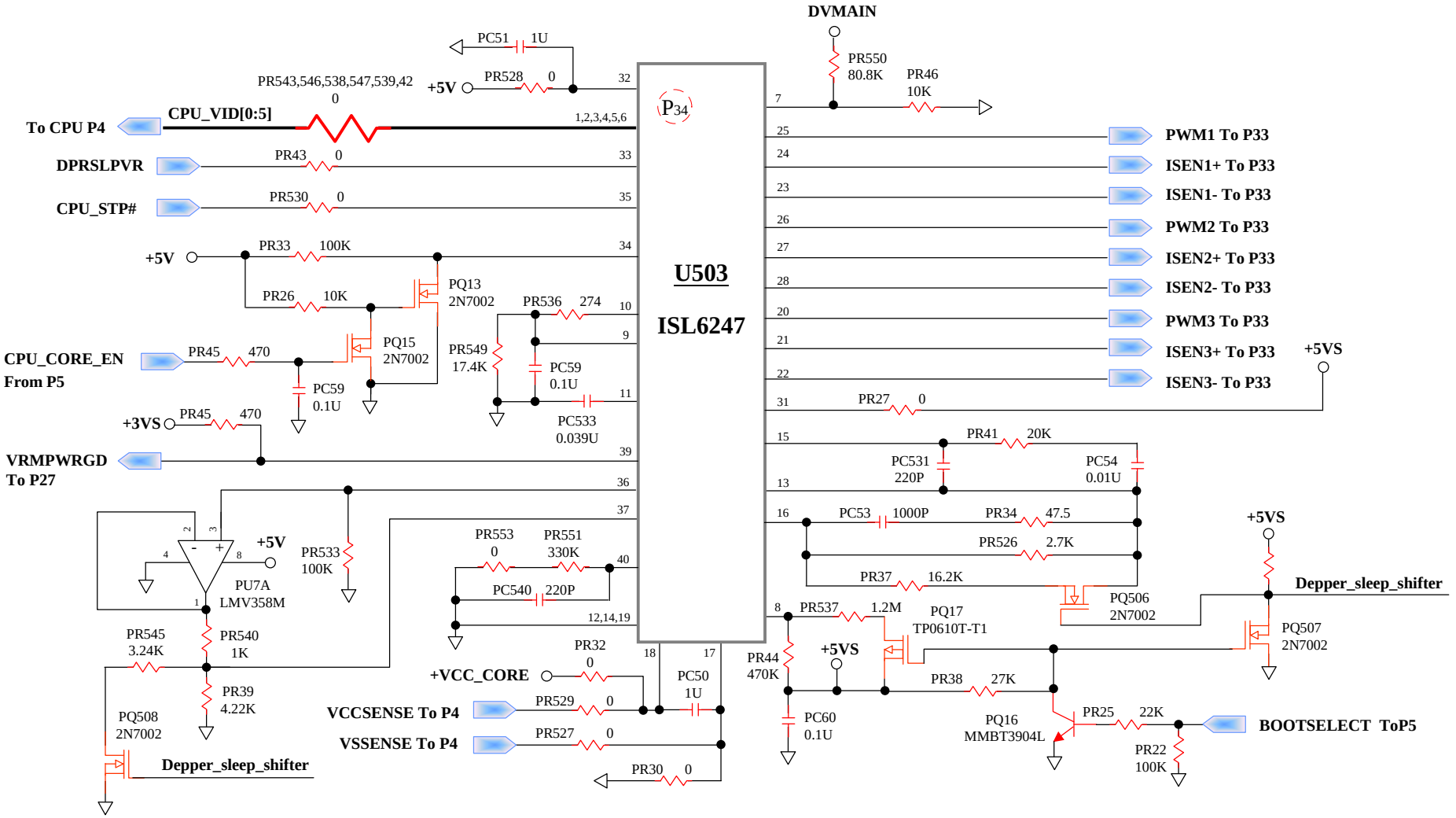


8555 N/B Maintenance

8.1 No Power– No CPU Core

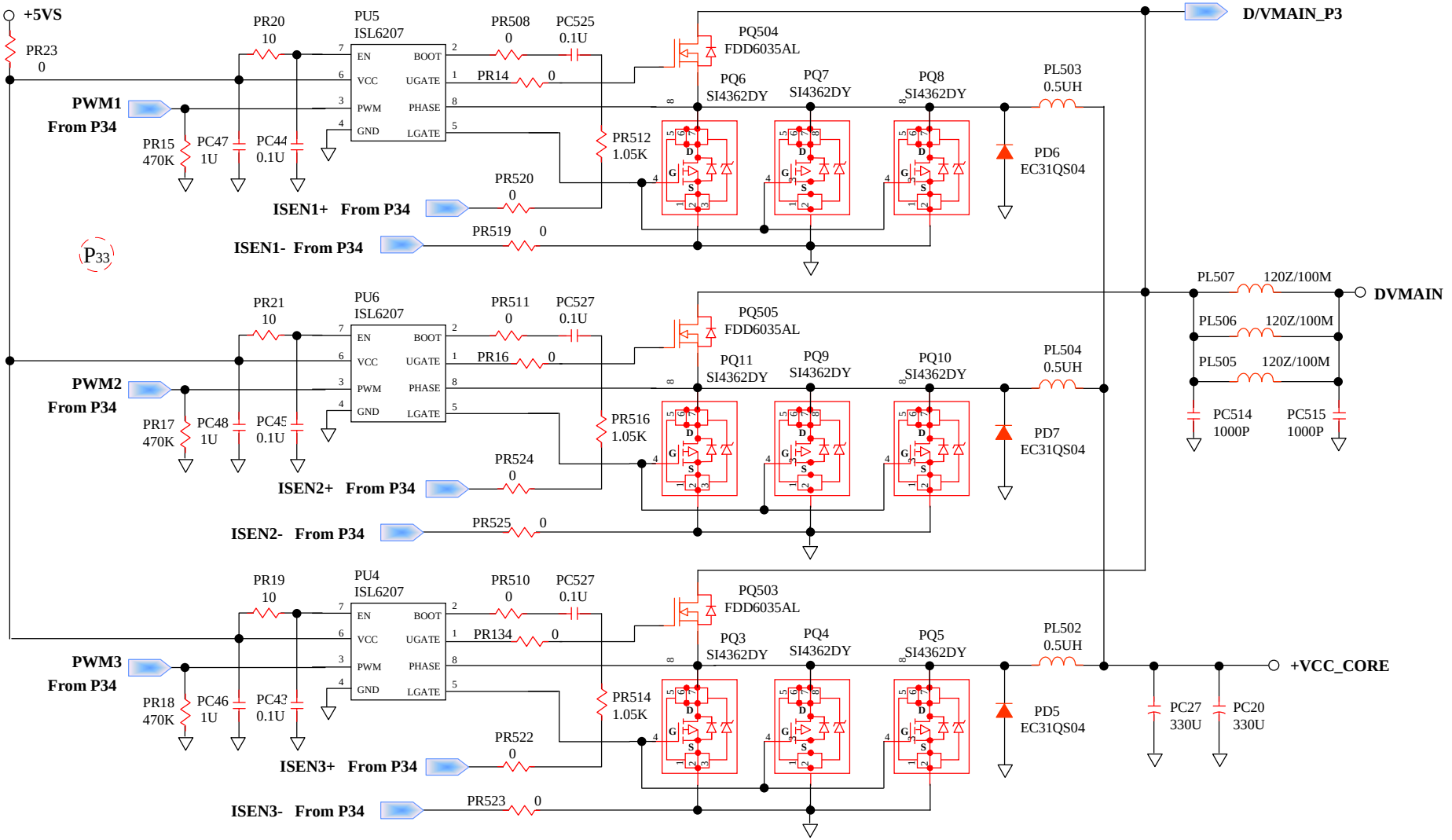
When the power button is pressed, nothing happens ,power indicator does not light up.And no CPU core.



8555 N/B Maintenance

8.1 No Power– No CPU Core

When the power button is pressed, nothing happens ,power indicator does not light up.And no CPU core.



8555 N/B Maintenance

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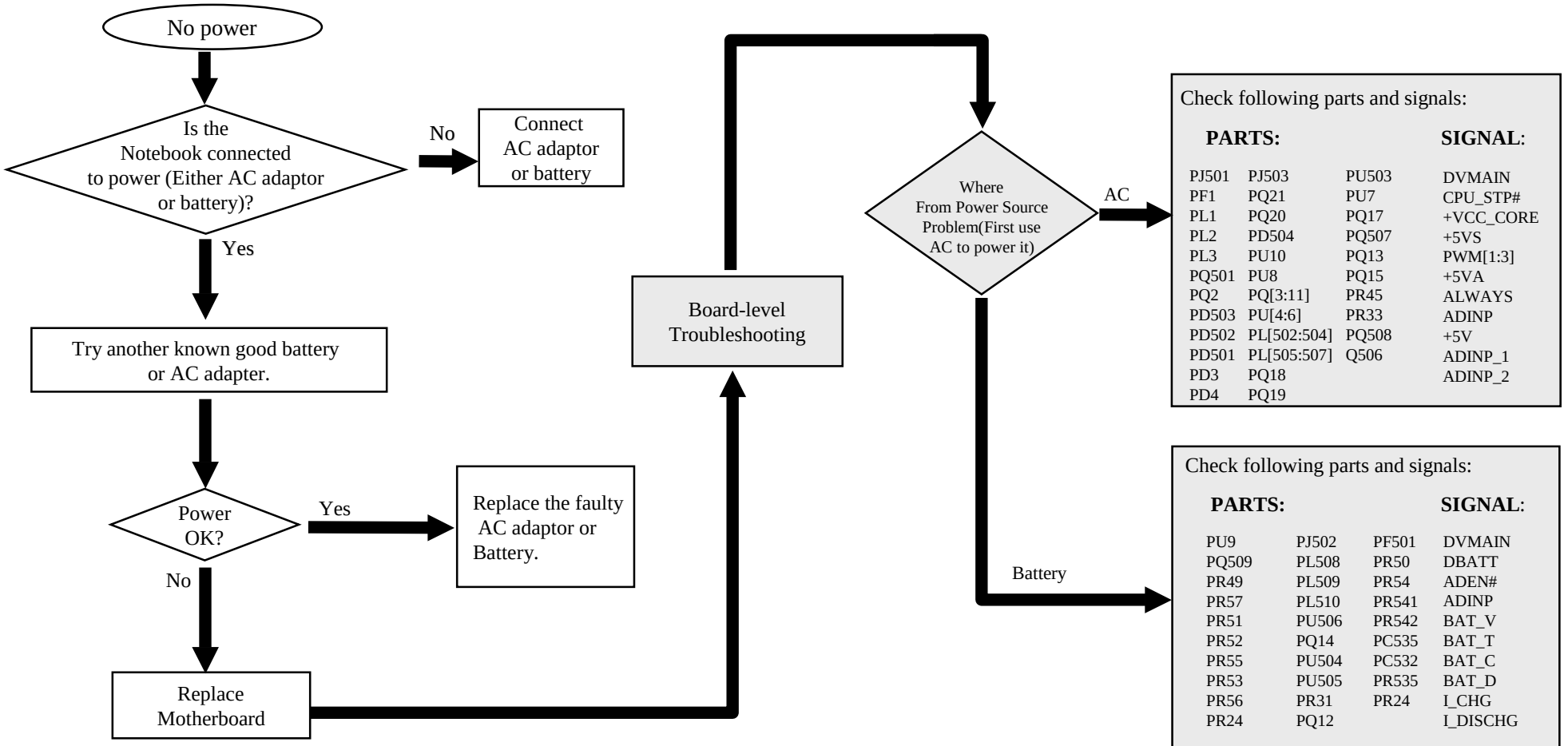
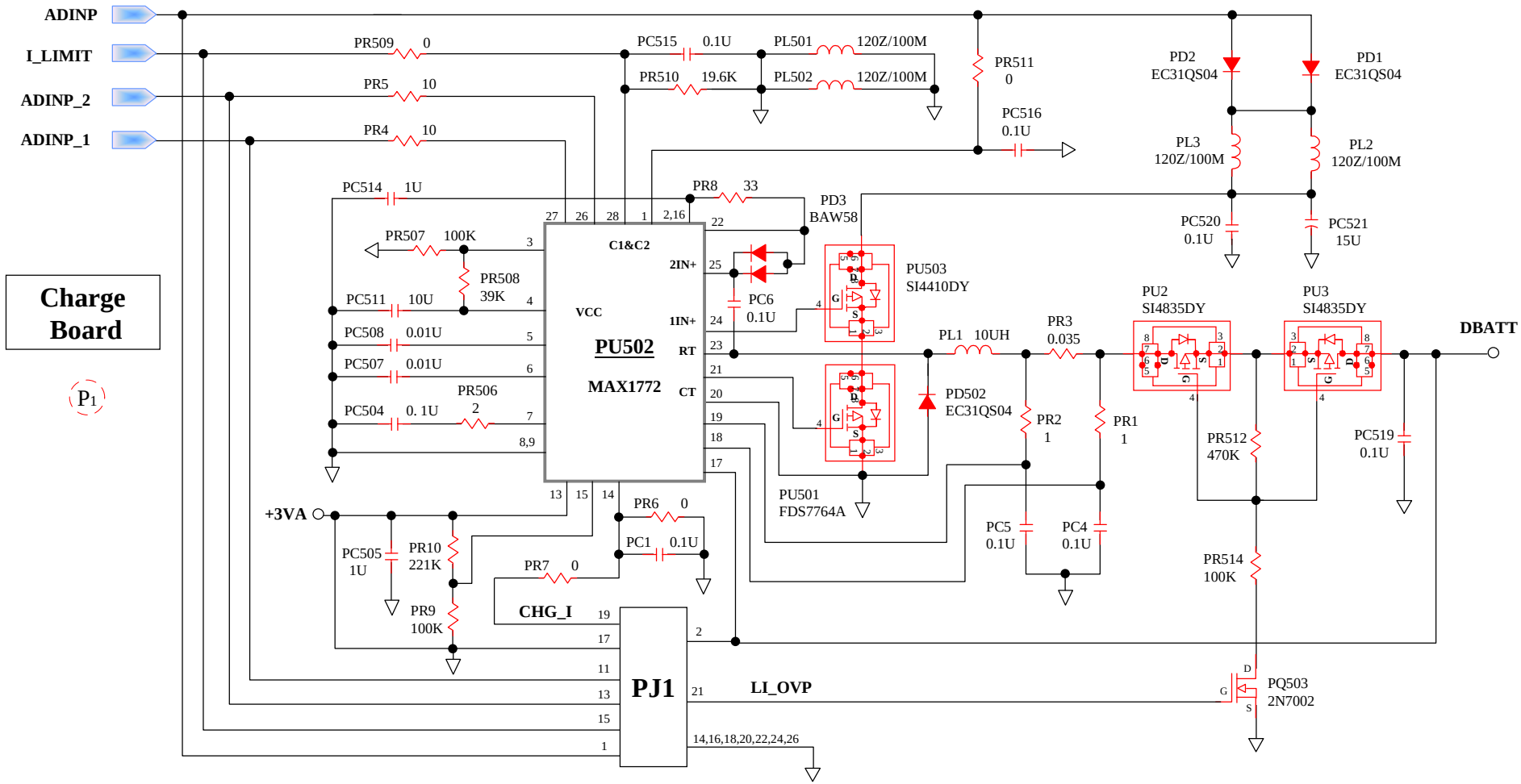


8555 N/B Maintenance

8.2 Battery Can not Be Charged

Symptom:

When the battery is installed but the battery status indicate LED display abnormal.



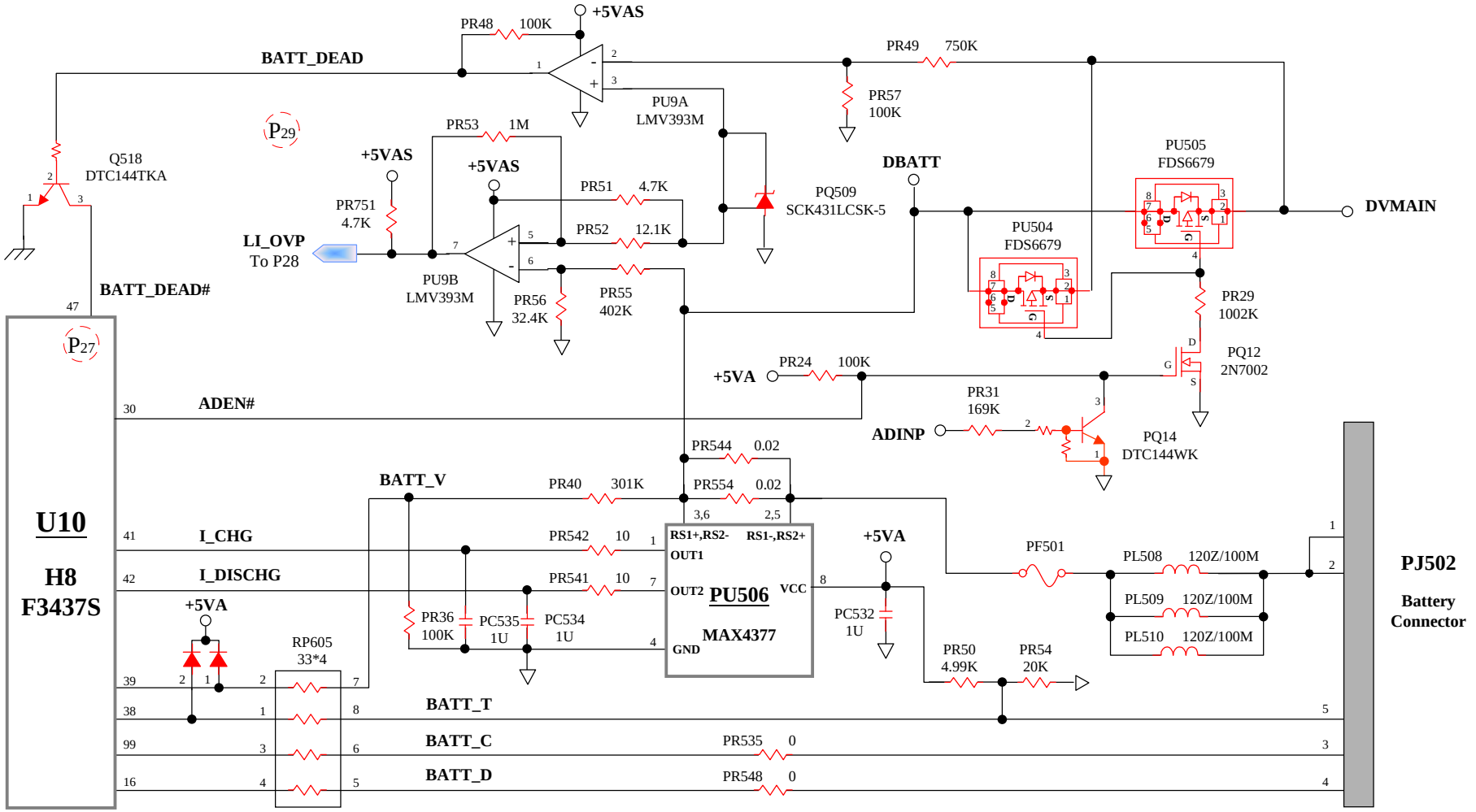
Connect to M/B

8555 N/B Maintenance

8.2 Battery Can not Be Charged

Symptom:

When the battery is installed but the battery status indicate LED display abnormal.



8555 N/B Maintenance

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Symptom:

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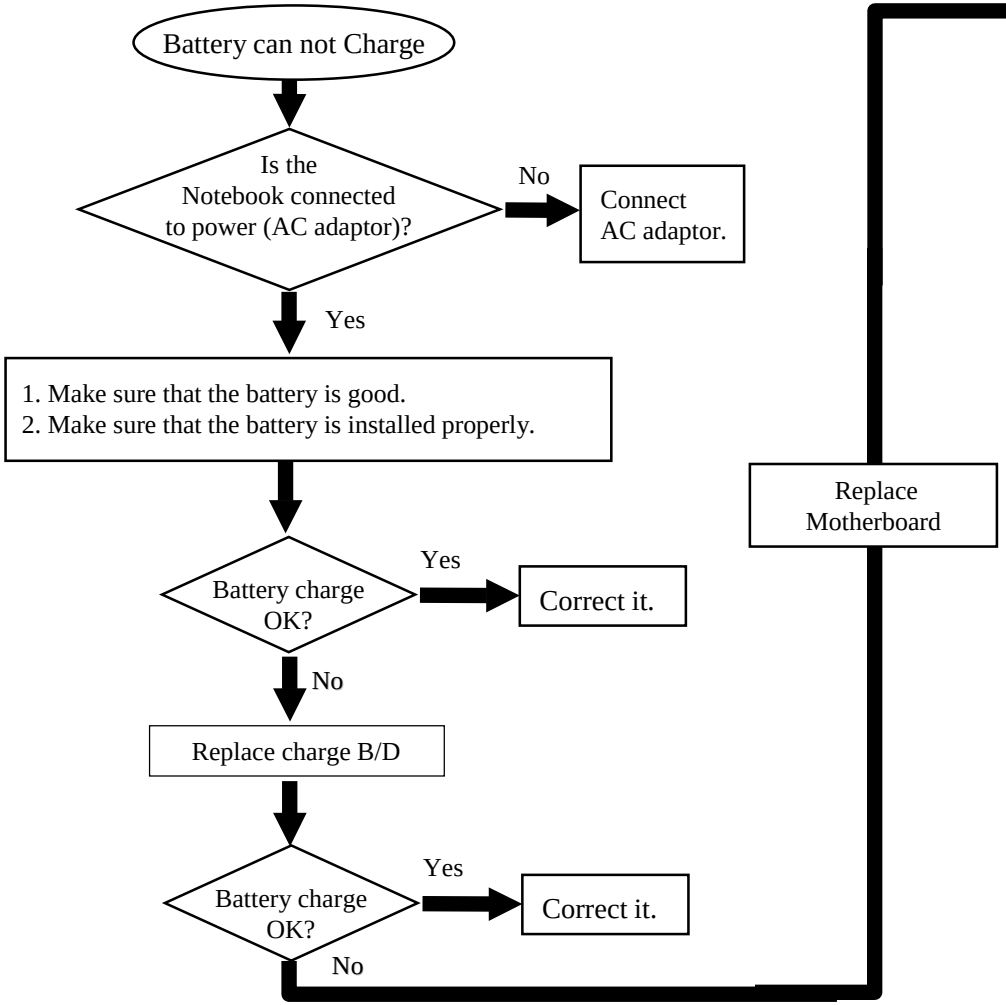
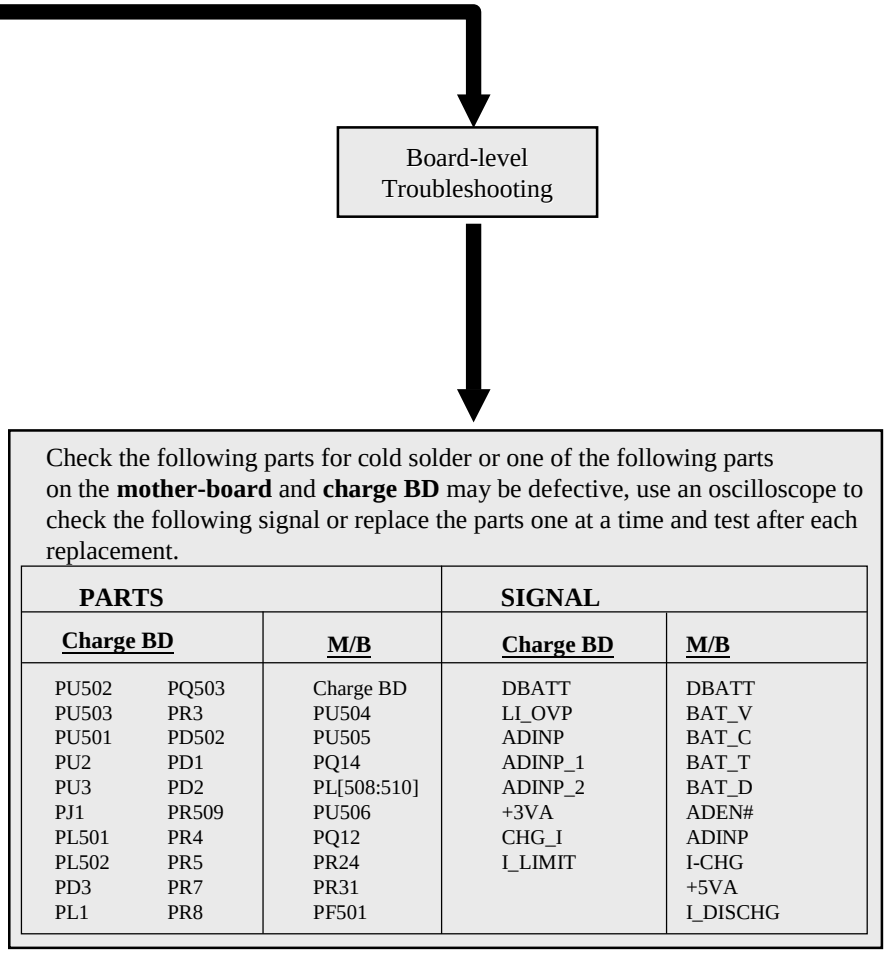




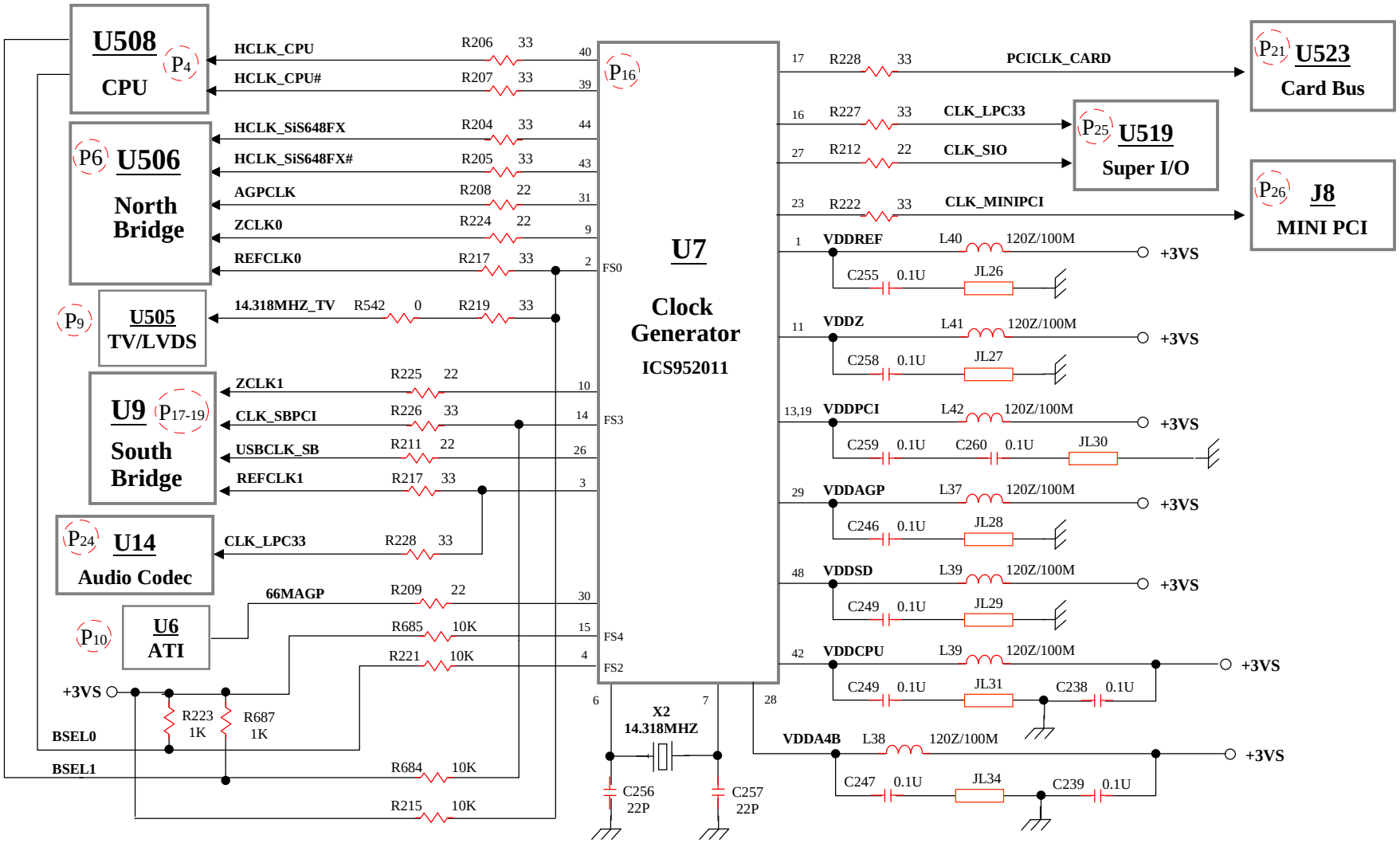
Check the following parts for cold solder or one of the following parts on the **mother-board** and **charge BD** may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

PARTS			**SIGNAL**	
Charge BD		**M/B**	**Charge BD**	**M/B**
PU502	PQ503	Charge BD	DBATT	DBATT
PU503	PR3	PU504	LI_OVP	BAT_V
PU501	PD502	PU505	ADINP	BAT_C
PU2	PD1	PQ14	ADINP_1	BAT_T
PU3	PD2	PL[508:510]	ADINP_2	BAT_D
PJ1	PR509	PU506	+3VA	ADEN#
PL501	PR4	PQ12	CHG_I	ADINP
PL502	PR5	PR24	I_LIMIT	I-CHG
PD3	PR7	PR31		+5VA
PL1	PR8	PF501		I_DISCHG

8555 N/B Maintenance

8.3 No Display (System Failure)

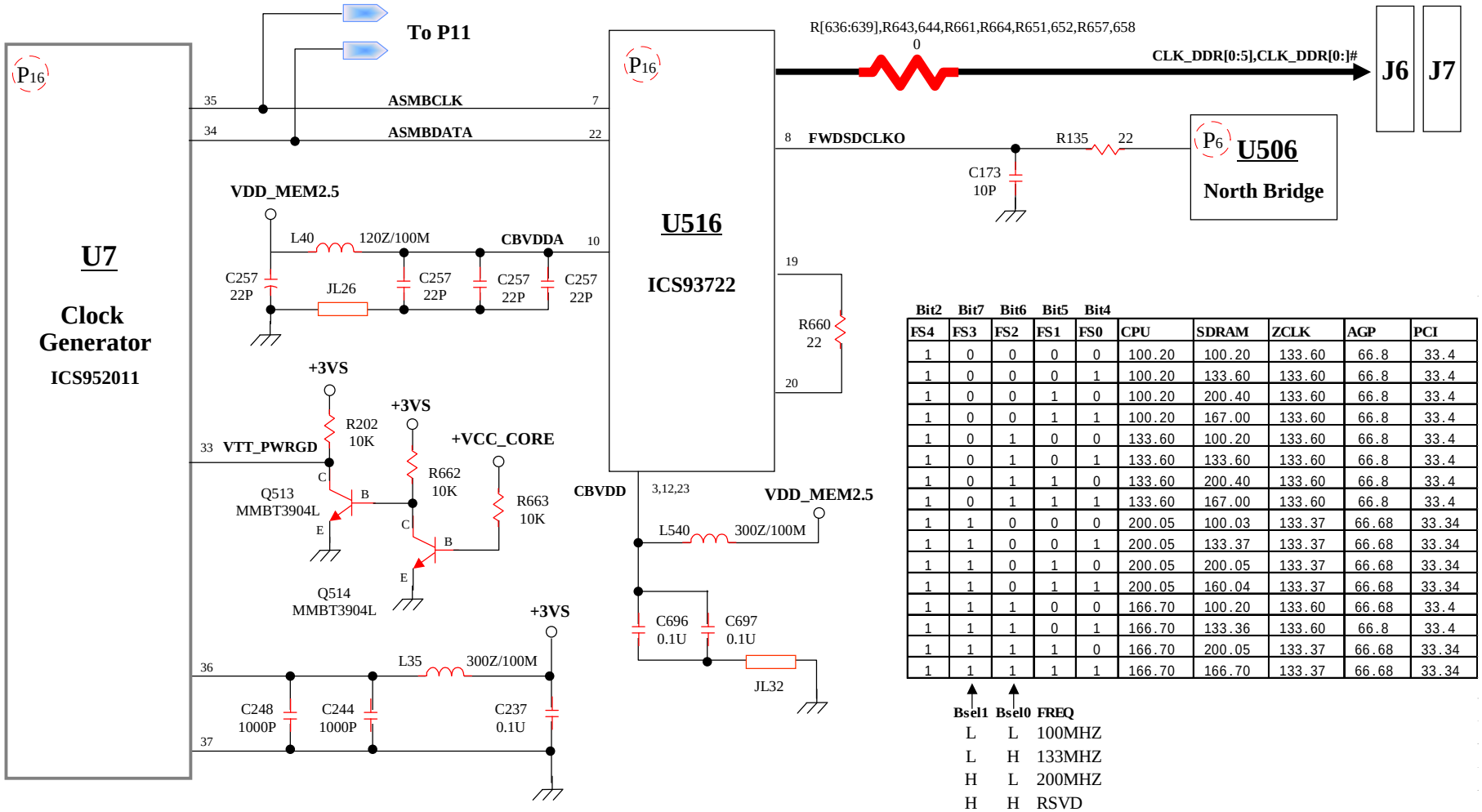
******System Clock Check******



8555 N/B Maintenance

8.3 No Display (System Failure)

******System Clock Check******



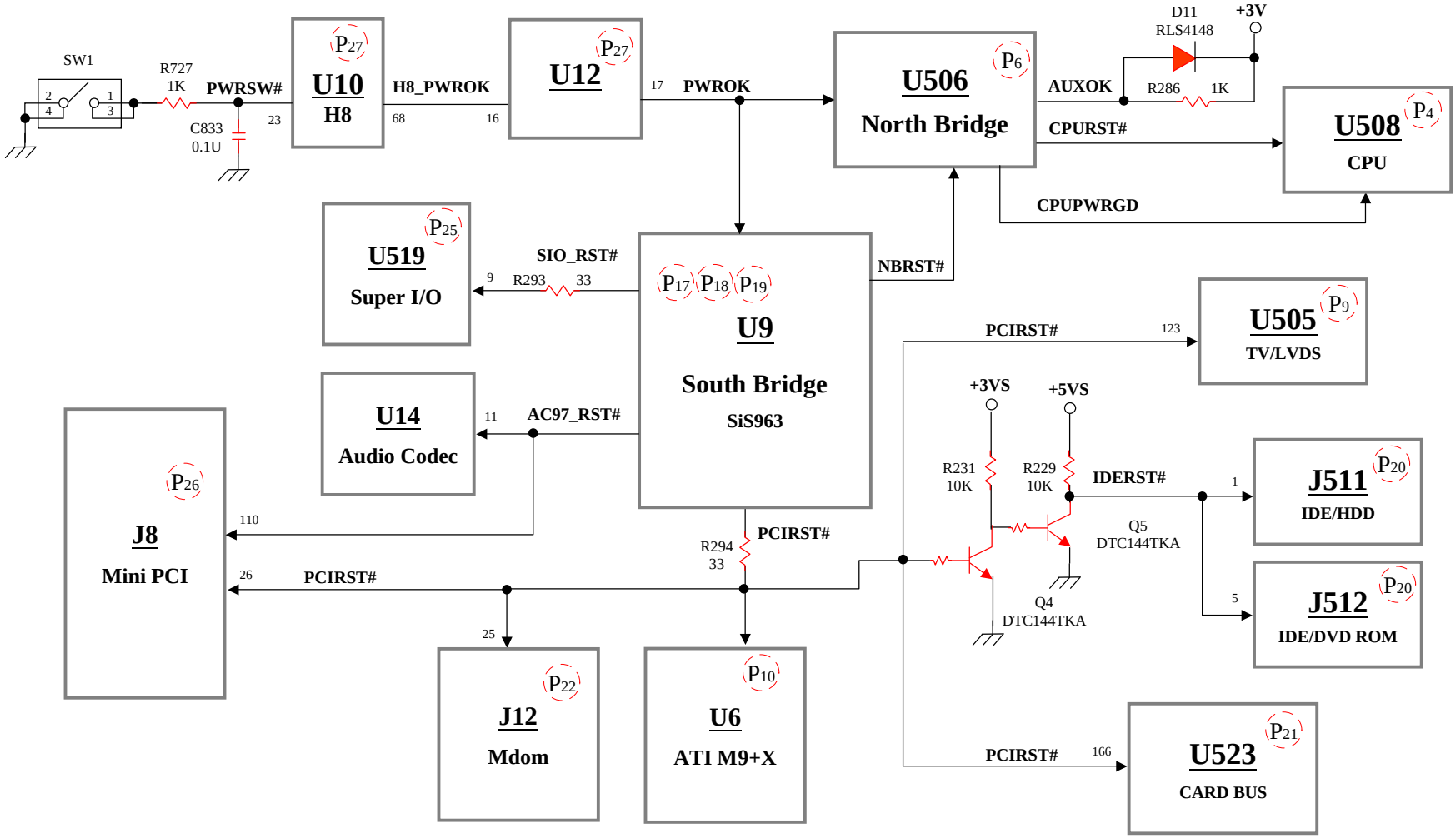
Bit2	Bit7	Bit6	Bit5	Bit4					
FS4	FS3	FS2	FS1	FS0	CPU	SDRAM	ZCLK	AGP	PCI
1	0	0	0	0	100.20	100.20	133.60	66.8	33.4
1	0	0	0	1	100.20	133.60	133.60	66.8	33.4
1	0	0	1	0	100.20	200.40	133.60	66.8	33.4
1	0	0	1	1	100.20	167.00	133.60	66.8	33.4
1	0	1	0	0	133.60	100.20	133.60	66.8	33.4
1	0	1	0	1	133.60	133.60	133.60	66.8	33.4
1	0	1	1	0	133.60	200.40	133.60	66.8	33.4
1	0	1	1	1	133.60	167.00	133.60	66.8	33.4
1	1	0	0	0	200.05	100.03	133.37	66.68	33.34
1	1	0	0	1	200.05	133.37	133.37	66.68	33.34
1	1	0	1	0	200.05	200.05	133.37	66.68	33.34
1	1	0	1	1	200.05	160.04	133.37	66.68	33.34
1	1	1	0	0	166.70	100.20	133.60	66.68	33.4
1	1	1	0	1	166.70	133.36	133.60	66.8	33.4
1	1	1	1	0	166.70	200.05	133.37	66.68	33.34
1	1	1	1	1	166.70	166.70	133.37	66.68	33.34

Bsel1	Bsel0	FREQ
L	L	100MHZ
L	H	133MHZ
H	L	200MHZ
H	H	RSVD

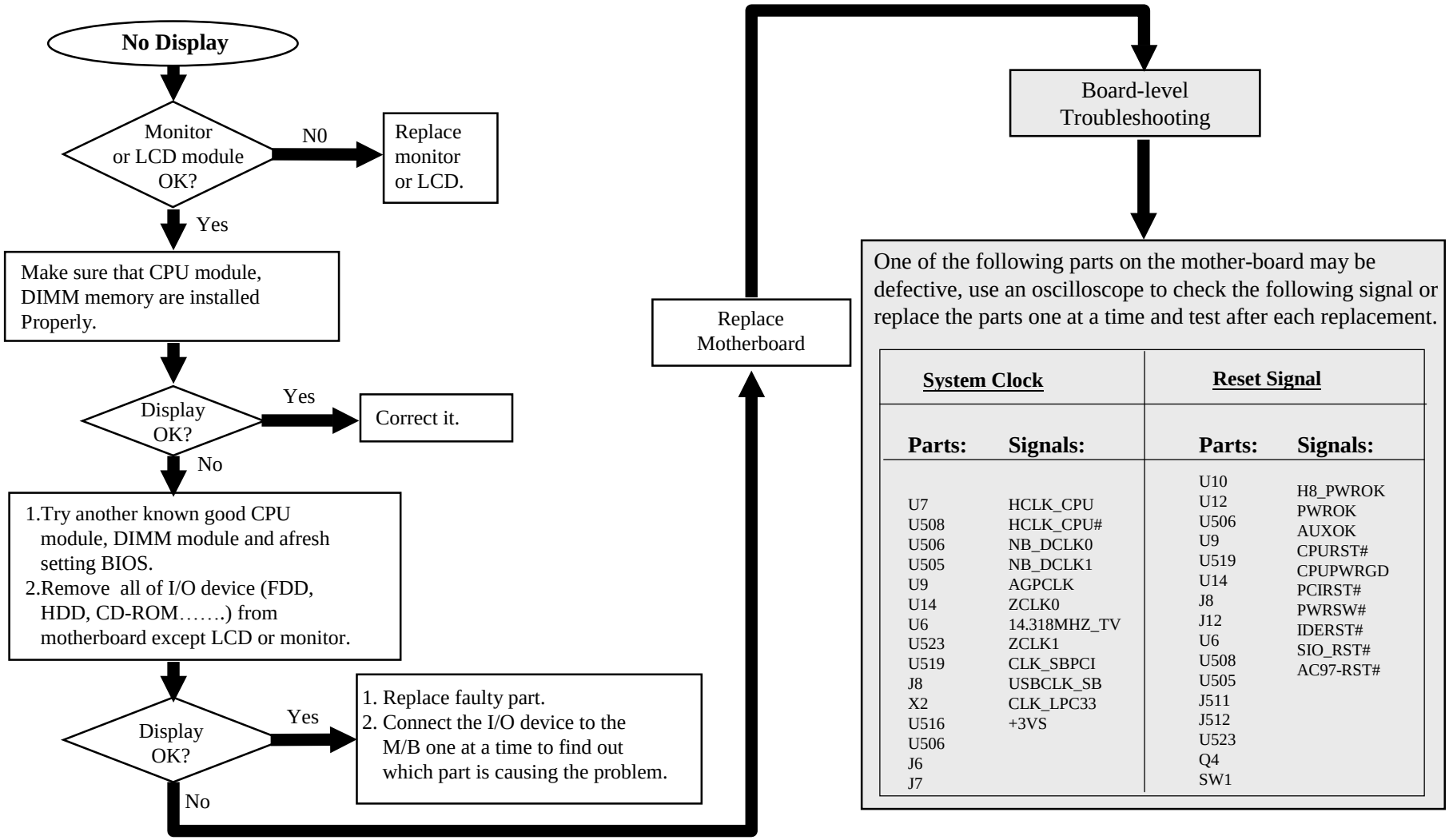
8555 N/B Maintenance

8.3 No Display (System Failure)

********Reset Circuit Checking********



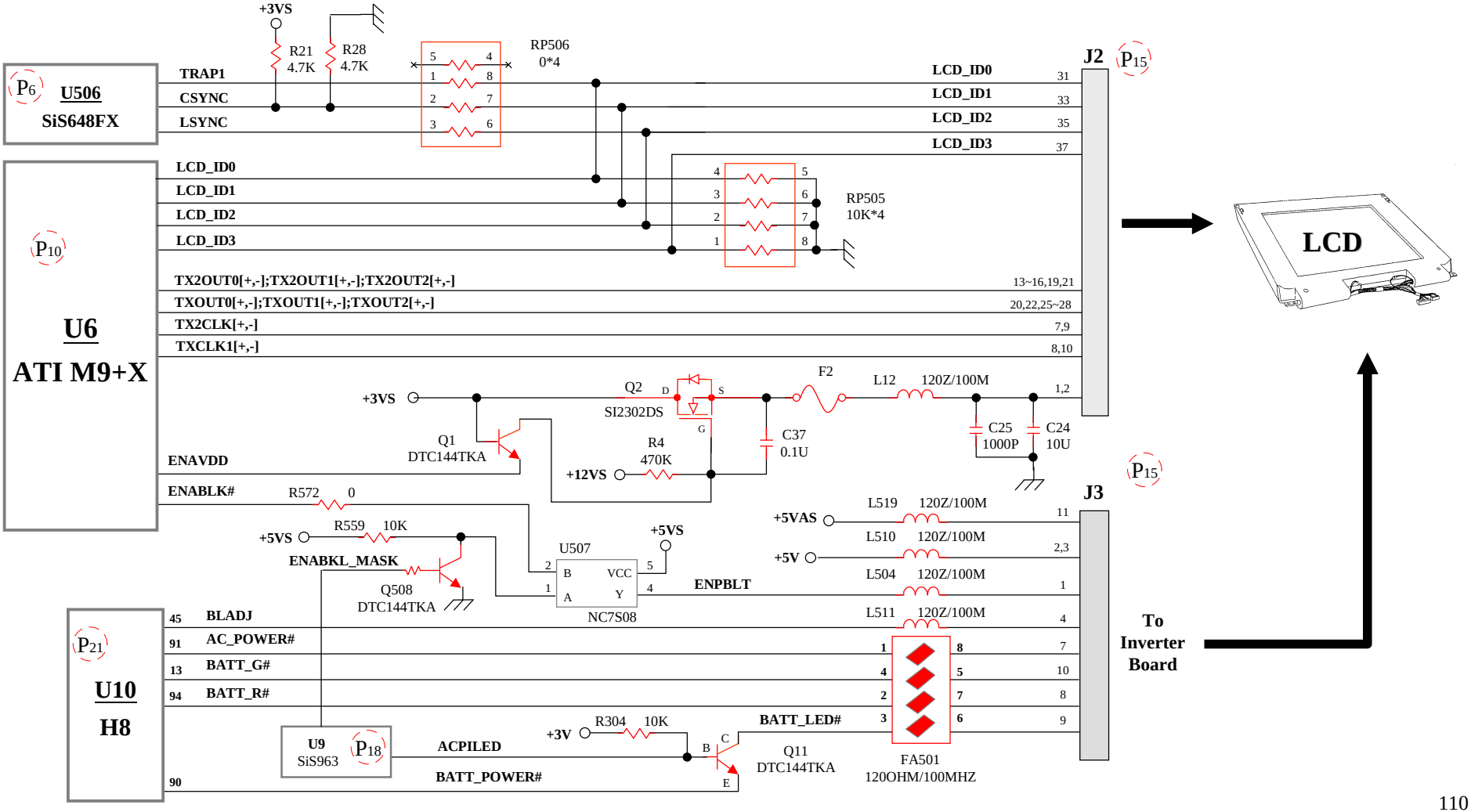
8.3 No Display (System Failure)



8.4 VGA Controller Failure LCD No Display

Symptom:

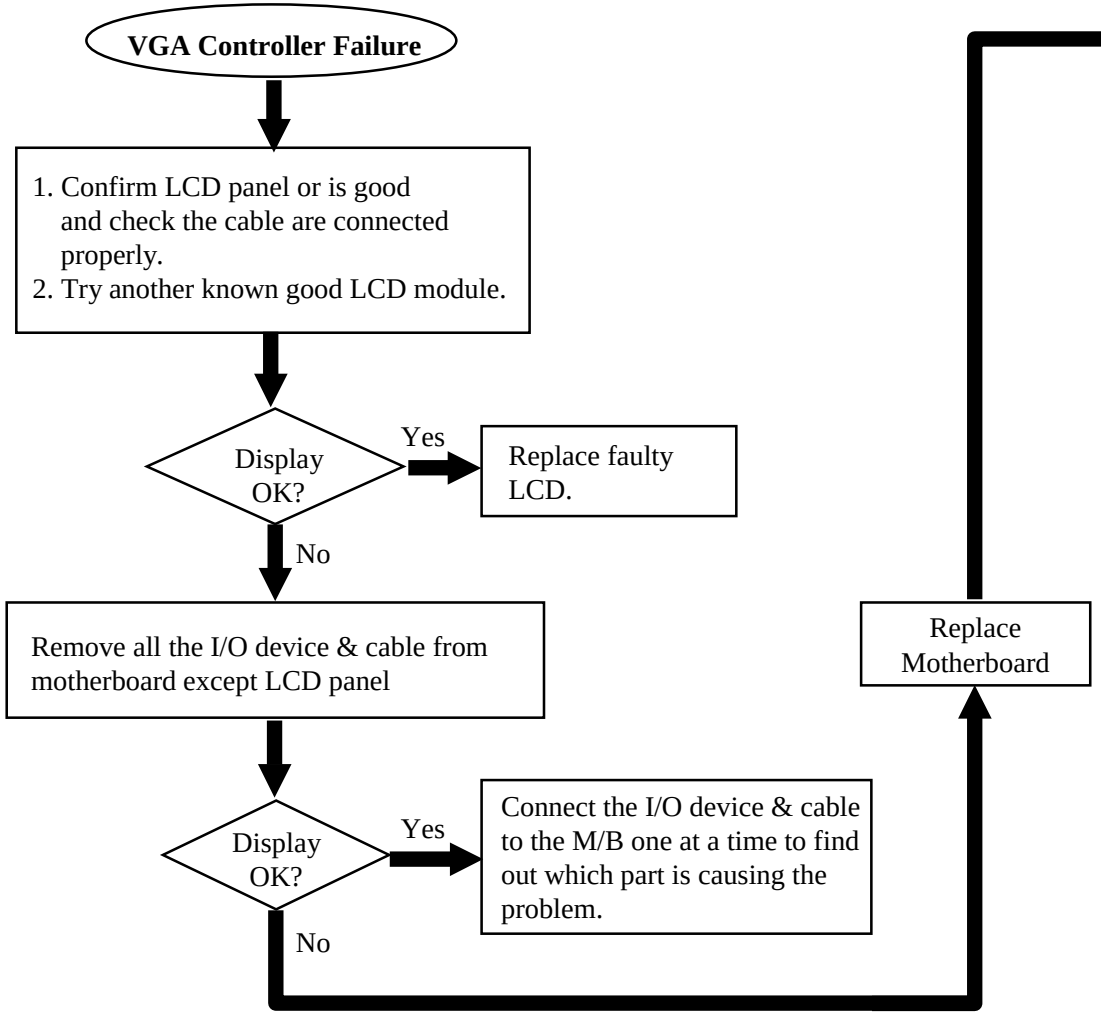
There is no display on LCD although power-on-self-test is passed.



8.4 VGA Controller Failure LCD No Display

Symptom:

There is no display on LCD although power-on-self-test is passed.


VGA Controller Failure
1. Confirm LCD panel or is good and check the cable are connected properly.
2. Try another known good LCD module.
Display OK?
Yes
Replace faulty LCD.
No
Remove all the I/O device & cable from motherboard except LCD panel
Display OK?
Yes
Connect the I/O device & cable to the M/B one at a time to find out which part is causing the problem.
No
Replace Motherboard
Board-level Troubleshooting

One of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

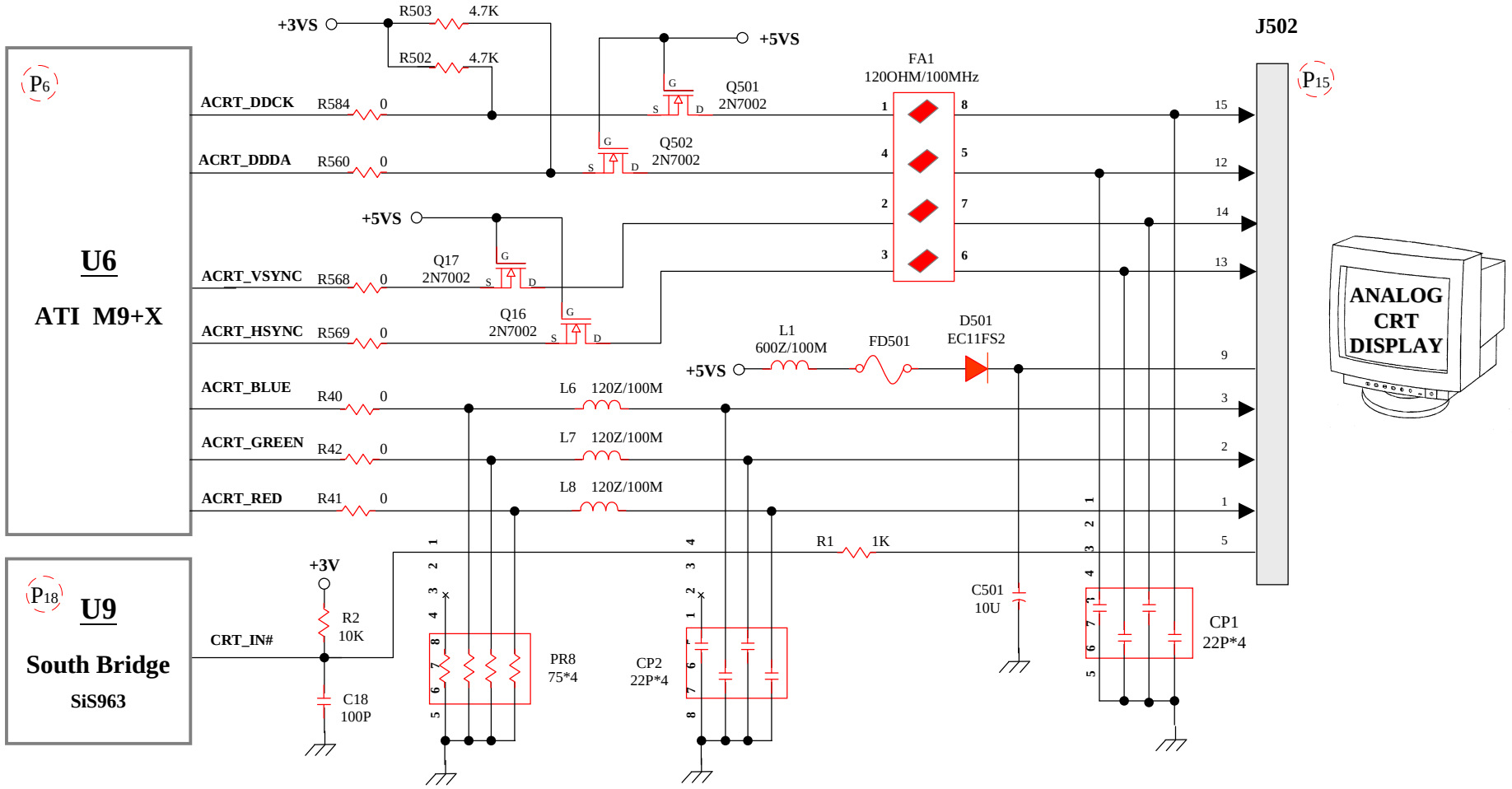
Parts:		**Signals:**	
U506	J3	TX2OUT0+,-	LCDID[0:3]
U6	U10	TX2OUT1+,-	LCD_ID[0:3]
RP506	Q11	TX2OUT2+,-	BATT_POWER#
RP505	FA501	TX2CLK+,-	TRAP1
Q2	U507	TXCLK+,-	CSYNC
F2	L519	ENAVDD	LSYNC
Q508	L510	ENABLK#	
U9	L504	BLADJ	
J2	L511	AC_POWER#	
		BATT_G#	
		BATT_R#	

8555 N/B Maintenance

8.5 External Monitor No Display

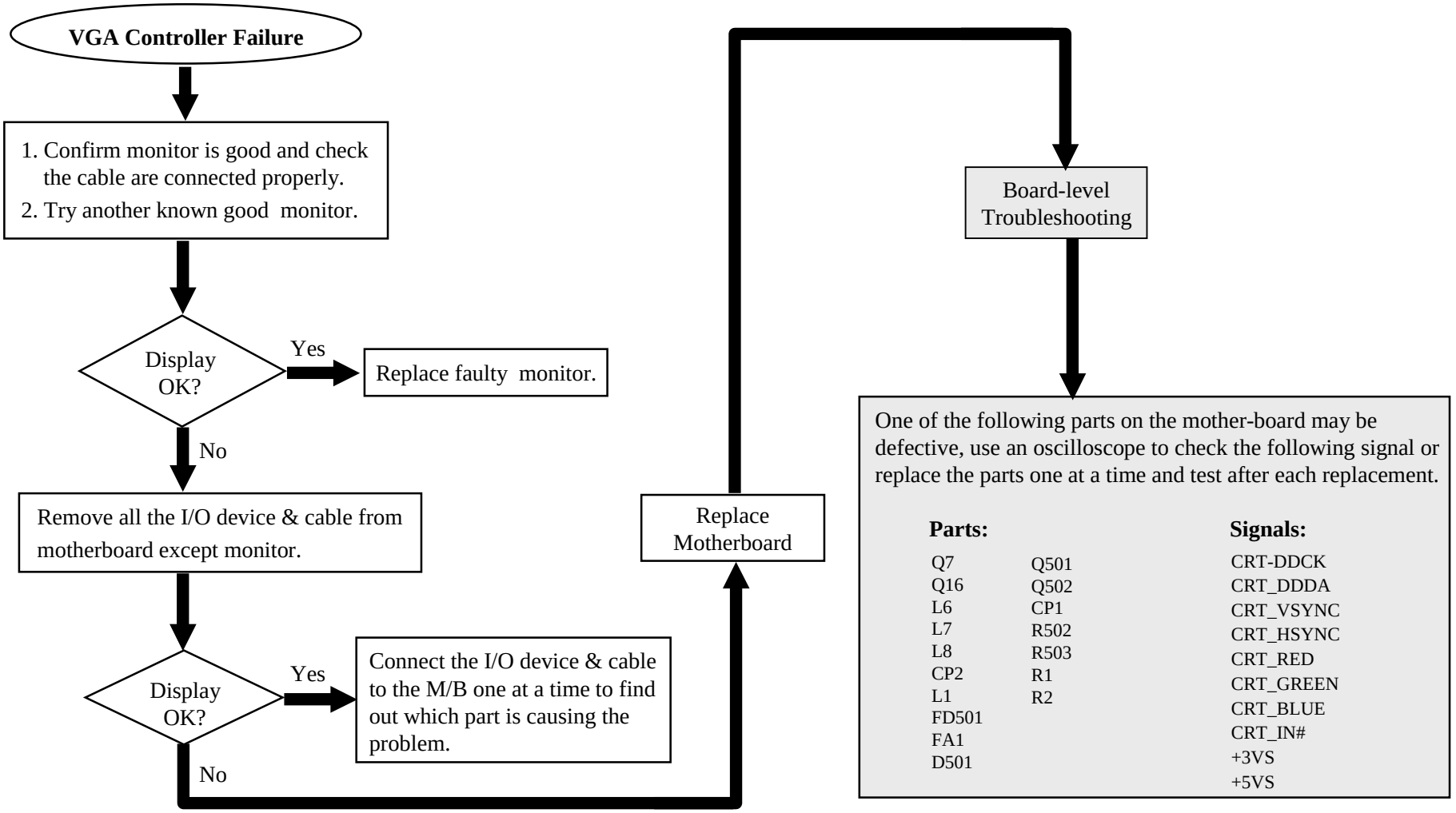
Symptom:

The CRT monitor shows nothing or abnormal color, but it is OK for LCD.



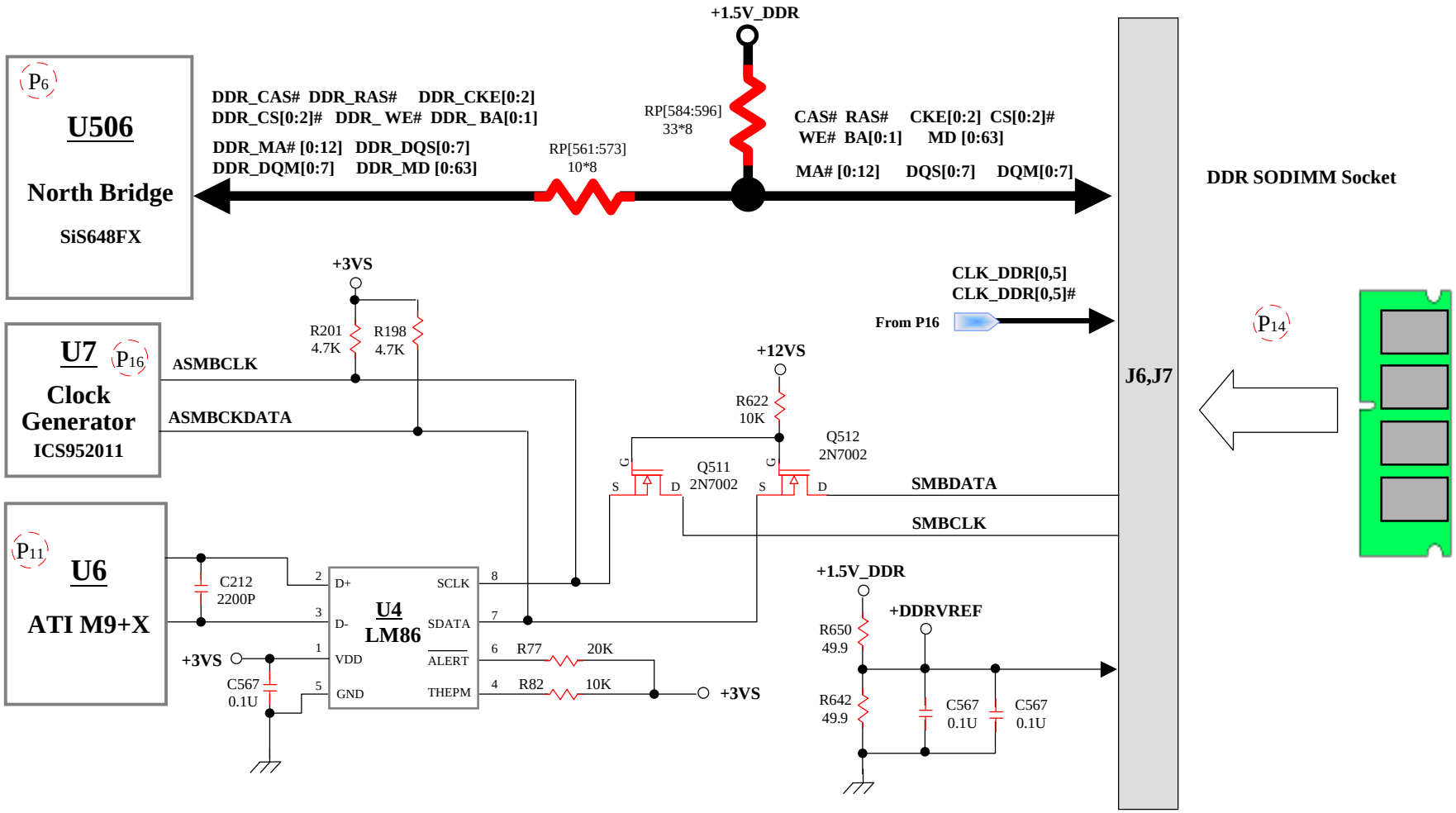
8.5 External Monitor No Display

Symptom:
The CRT monitor shows nothing or abnormal color, but it is OK for LCD.



8.6 Memory Test Error

Symptom:
Either on board or extend DDR RAM is failure or system hangs up.



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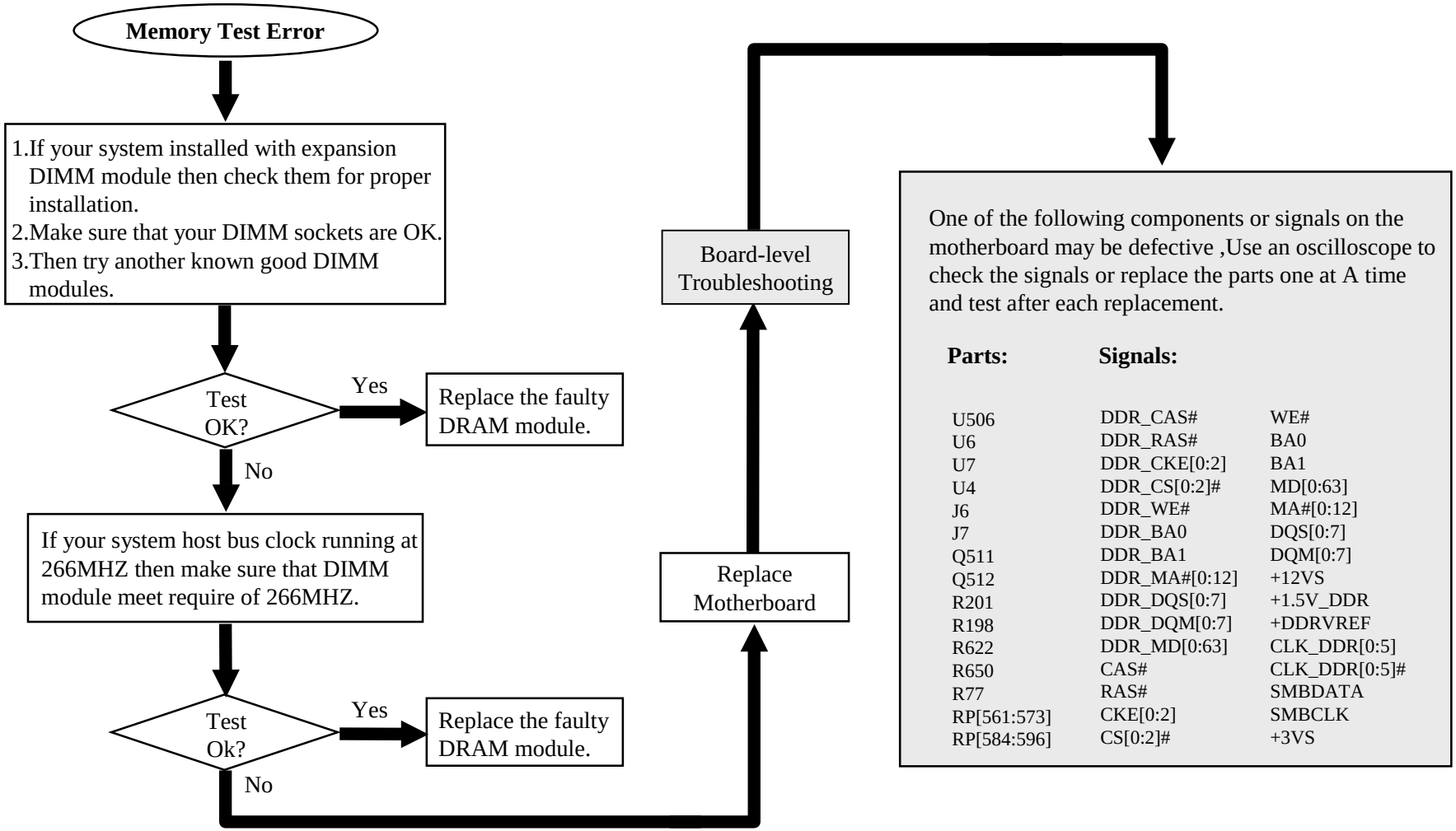
Symptom:
Either on board or extend DDR RAM is failure or system hangs up.

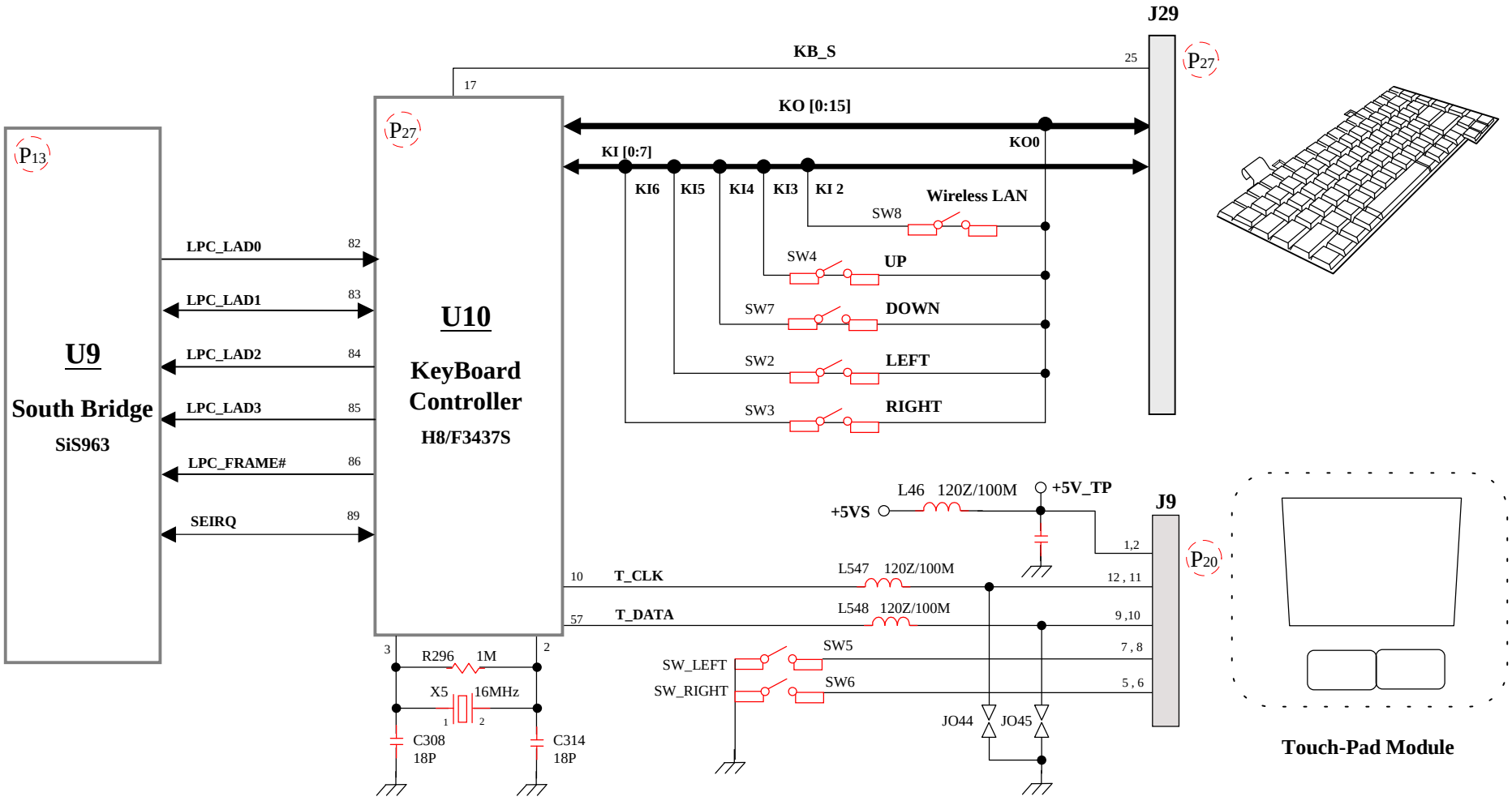


8555 N/B Maintenance

8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error

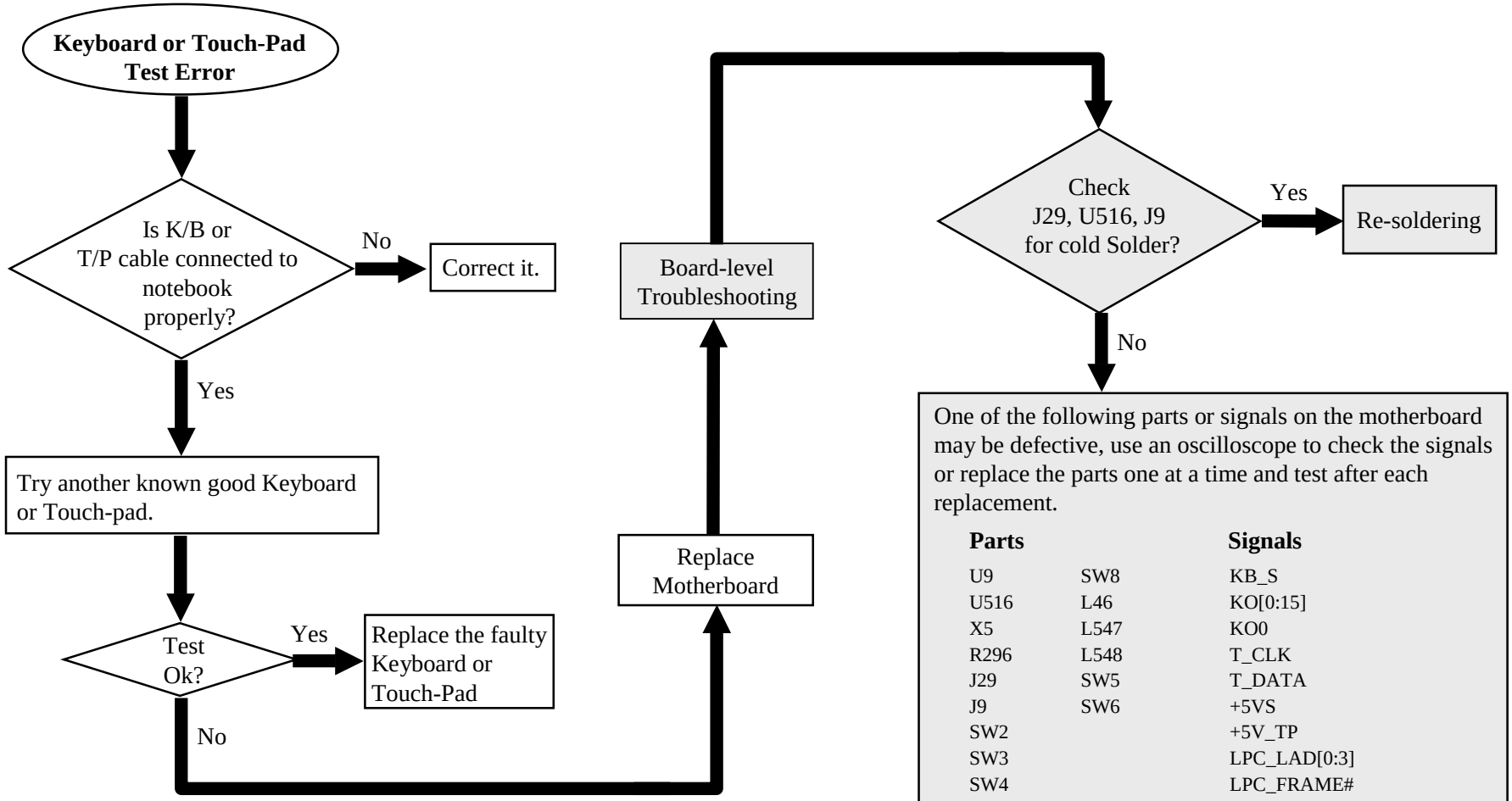
Symptom:

Error message of keyboard or touch-pad failure is shown or any key does not work.



8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error

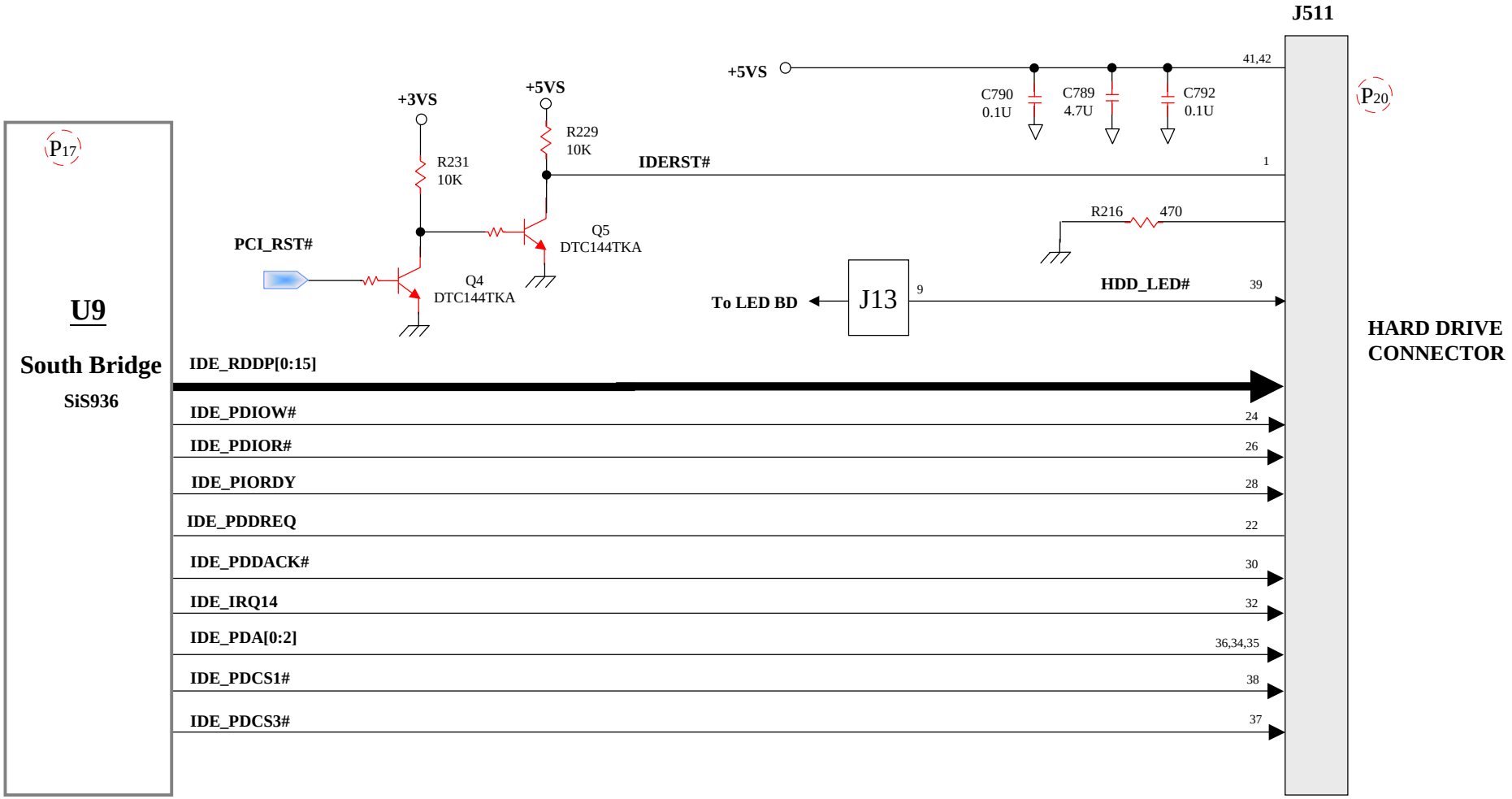
Symptom:
Error message of keyboard or touch-pad failure is shown or any key does not work.



8.8 Hard Disk Driver Test Error

Symptom:

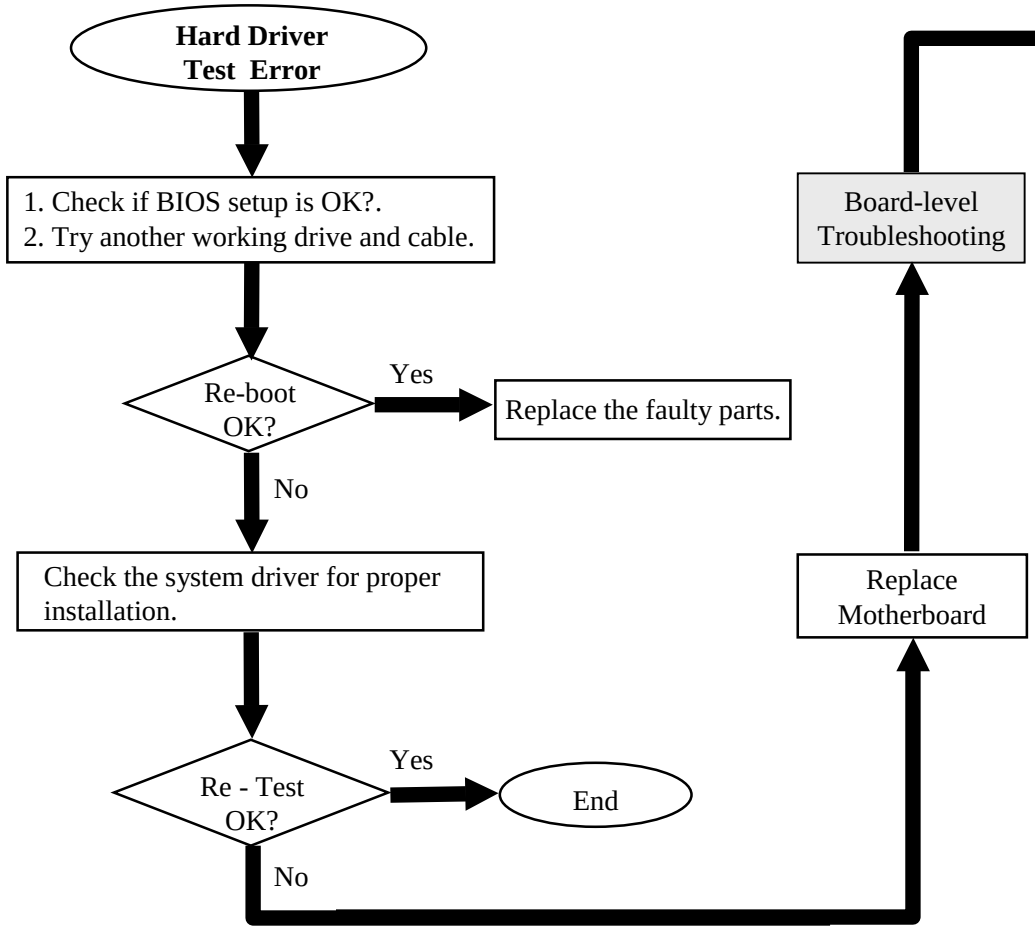
Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard-disk.



8.8 Hard Disk Driver Test Error

Symptom:

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard-disk.



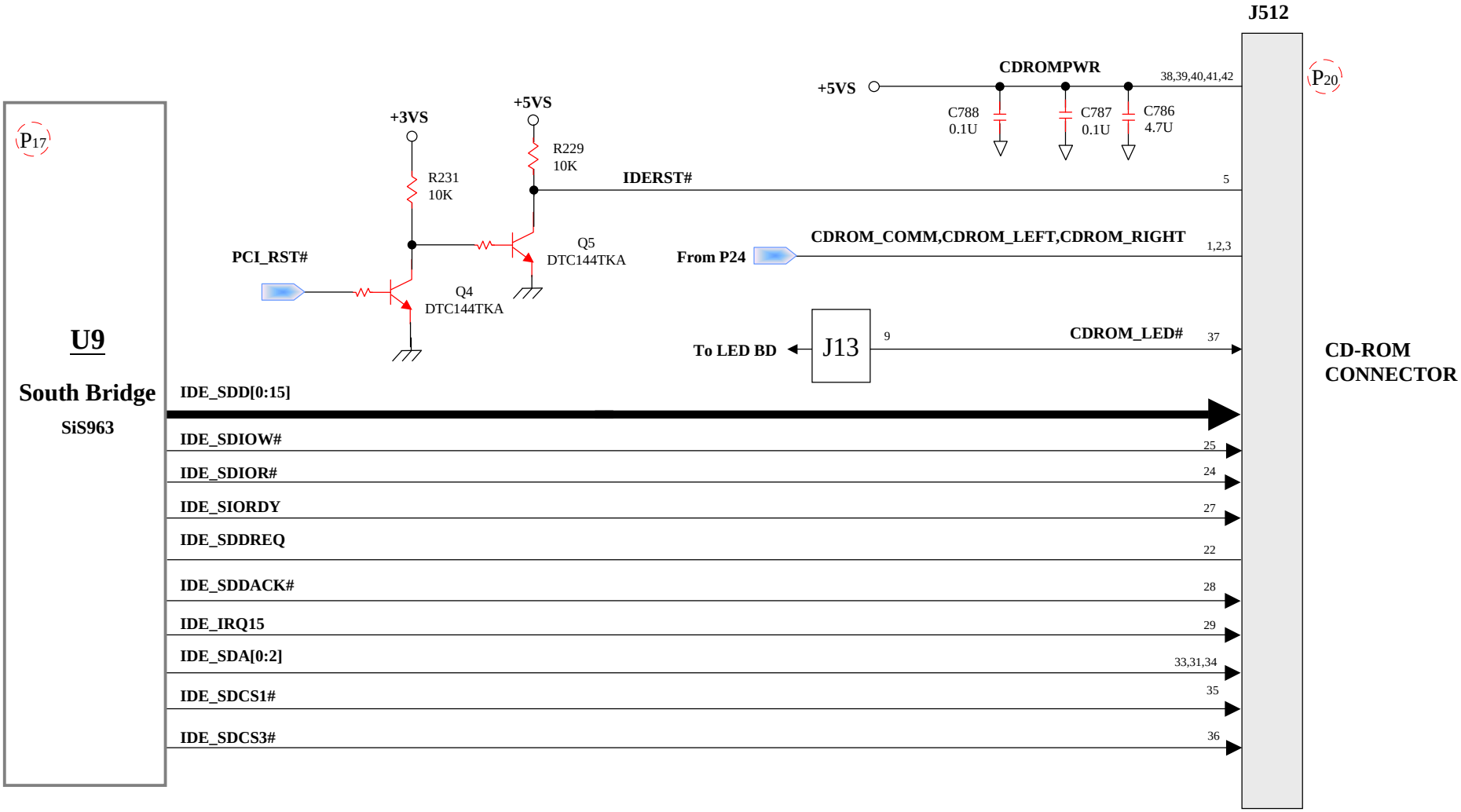
One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

PARTS:	SIGNALS:
U9	IDE_RDDP[0:15]
J511	IDE_PDIOW#
J13	IDE_PDIOR#
Q4	IDE_PIORDY
Q5	IDE_PDDREQ
R231	IDE_PDDACK#
R229	IDE_IRQ14
R216	IDE_PDA[0:2]
C790	IDE_PDCS1#
C789	IDE_PDCS3#
C792	+3VS
	+5VS
	PCI_RST#
	IDERST#
	HDD_LED#

8.9 CD-ROM Driver Test Error

Symptom:

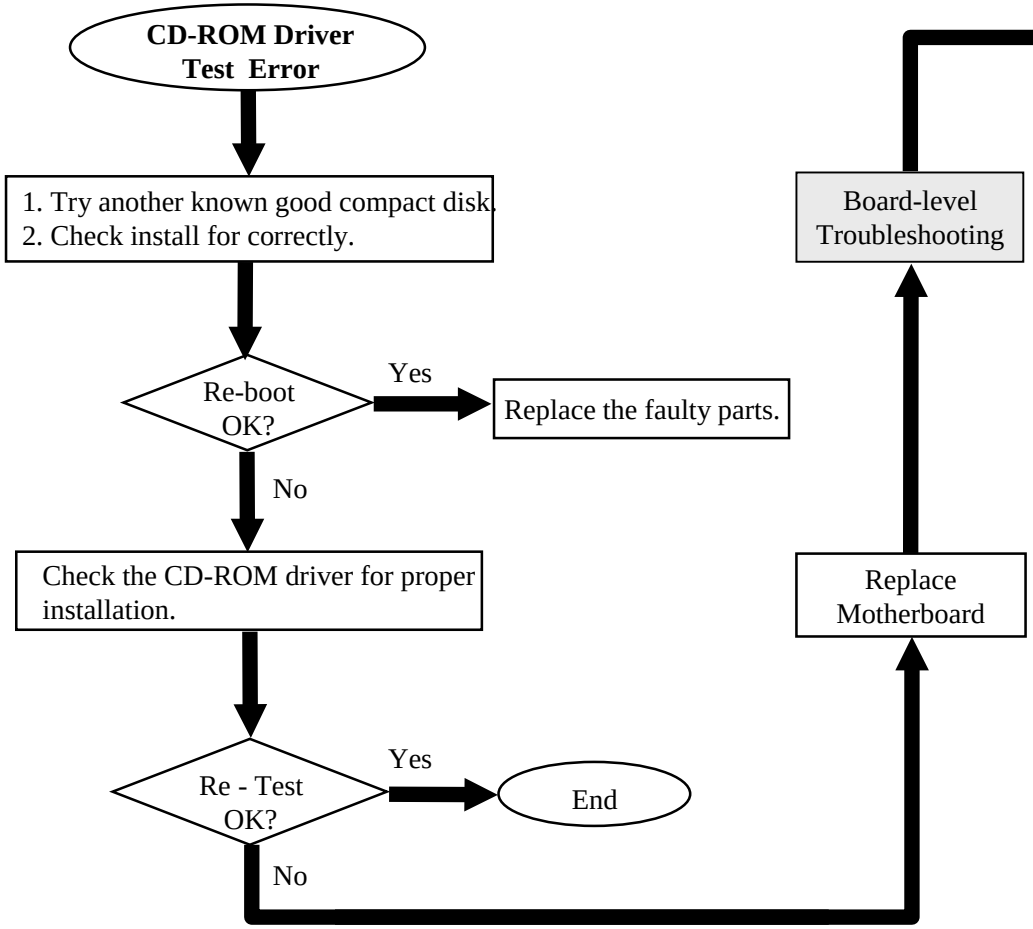
An error message is shown when reading data from CD-ROM drive.



8.9 CD-ROM Driver Test Error

Symptom:

An error message is shown when reading data from CD-ROM drive.

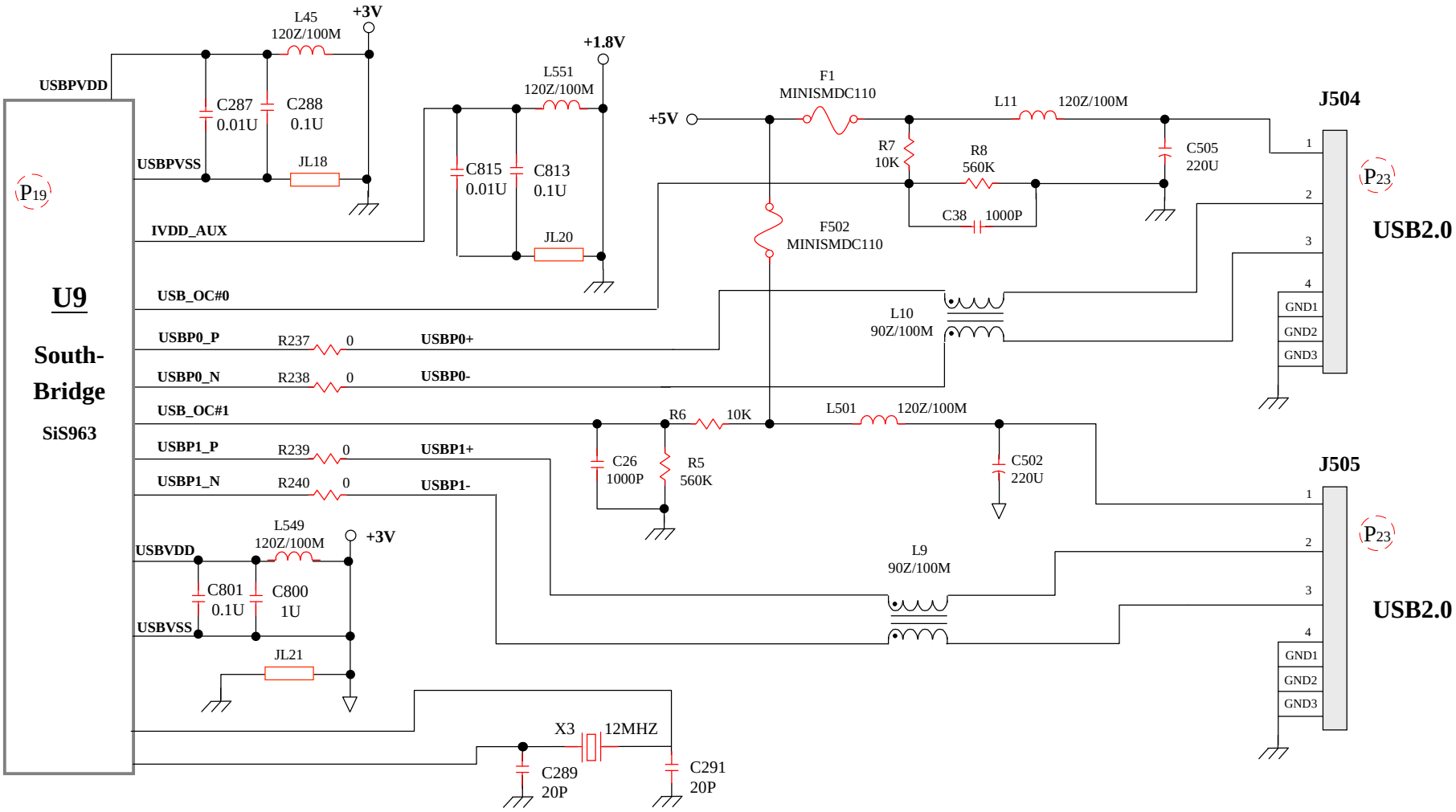


One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

PARTS:	SIGNALS:
U9	IDE_SDD[0:15]
J512	IDE_SDIOW#
Q4	IDE_SDIOR#
Q5	IDE_SIORDY
R231	IDE_SDDREQ
R229	IDE_SDDACK#
C786	IDE_IRQ15
C787	IDE_SDA[0:2]
C788	IDE_SDCS1#
J13	IDE_SDCS3#
	CDROMPWR
	IDERST#
	CDROM_COMM
	CDROM_RIGHT
	CDROM_LEFT
	CDROM_LED

8.10 USB2.0 Test Error (1)

Symptom:
An error occurs when a USB2.0 I/O device is installed.



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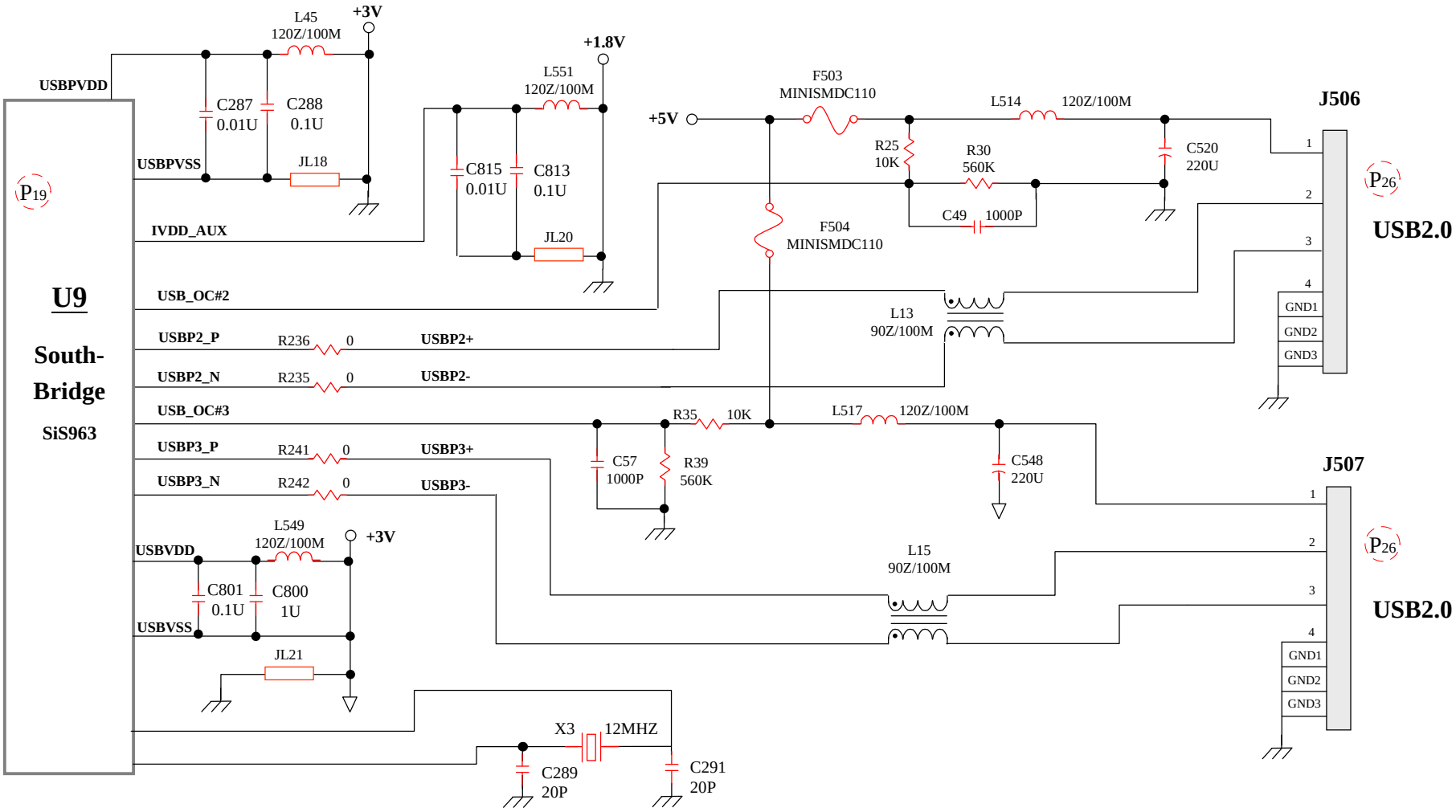
8.10 USB2.0 Test Error (2)

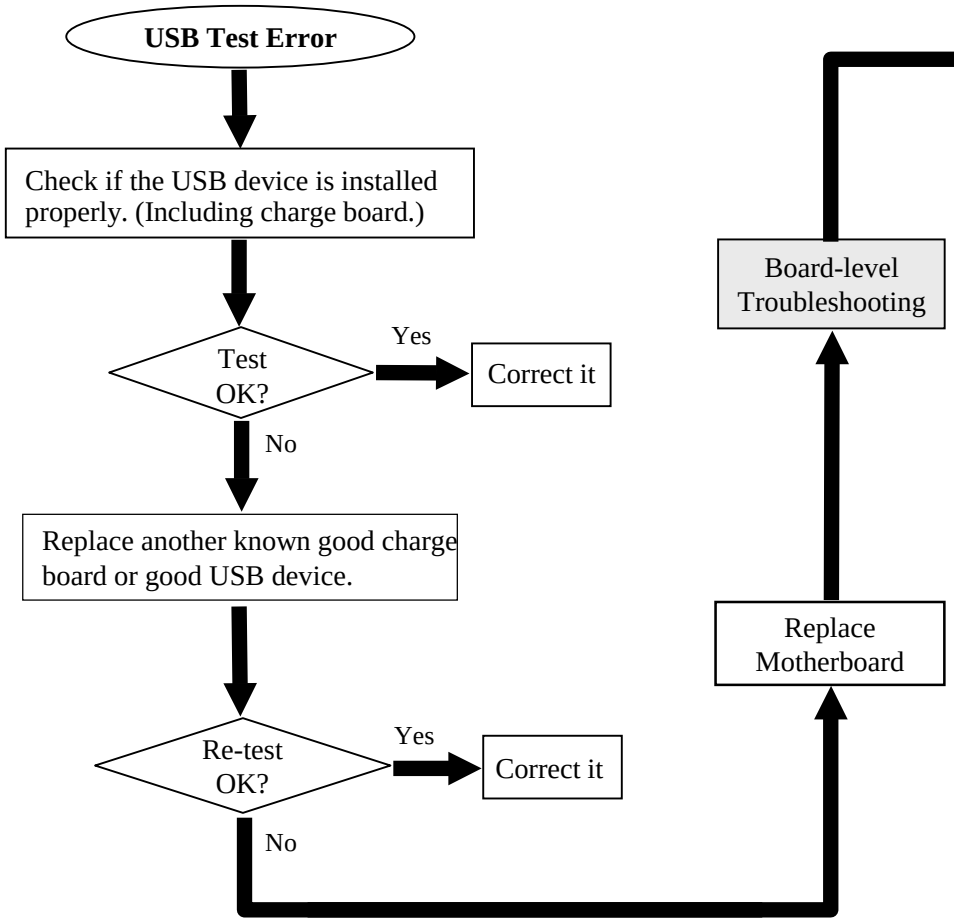
Symptom:

An error occurs when a USB I/O device is installed.



8.10 USB2.0 Test Error

Symptom:
An error occurs when a USB I/O device is installed.



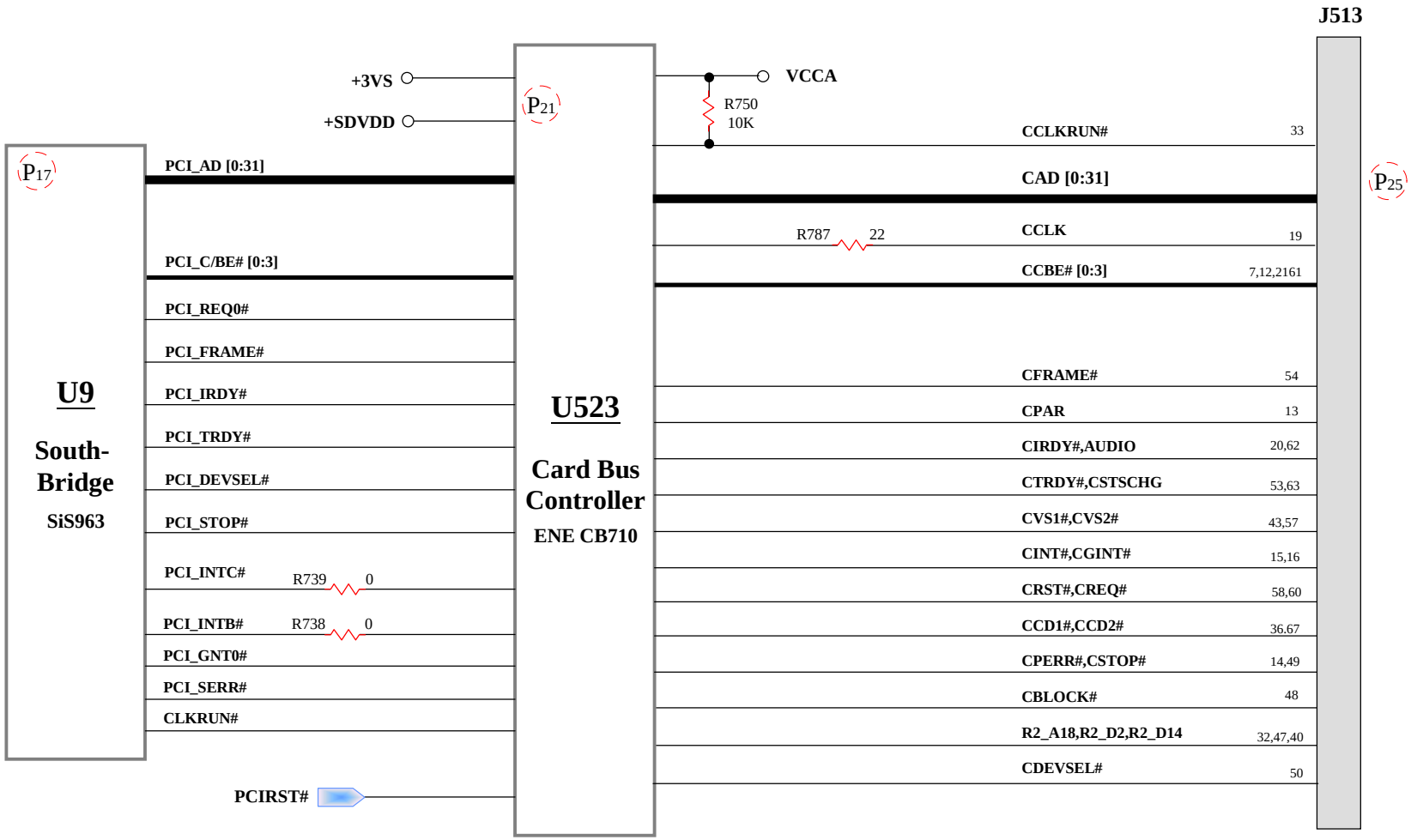
Check the following parts for cold solder or one of the following parts on the MB and Charge BD may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:			Signals:	
U9	F503	R8	+5V	USBP3-
J504	F504	C38	USB_OC#1	USBP3+
J505	L514	C26	USBP1-	USBVDD
J506	L517	C505	USBP1+	USBVSS
J507	L13	C49	USBOC#0	USBPVDD
F502	L15	C800	USBPO+	USBPVSS
F1	R25	C801	USBP0-	+1.8V
L501	R30	C57	USBP2-	
L9	R35	C505	USBP2+	
L11	R39	C287	USBOC#2	
L10	R6	C288	USBOC#3	
L549	R5			
X3	R7			

8.11 PC-Card Socket Failure

Symptom :

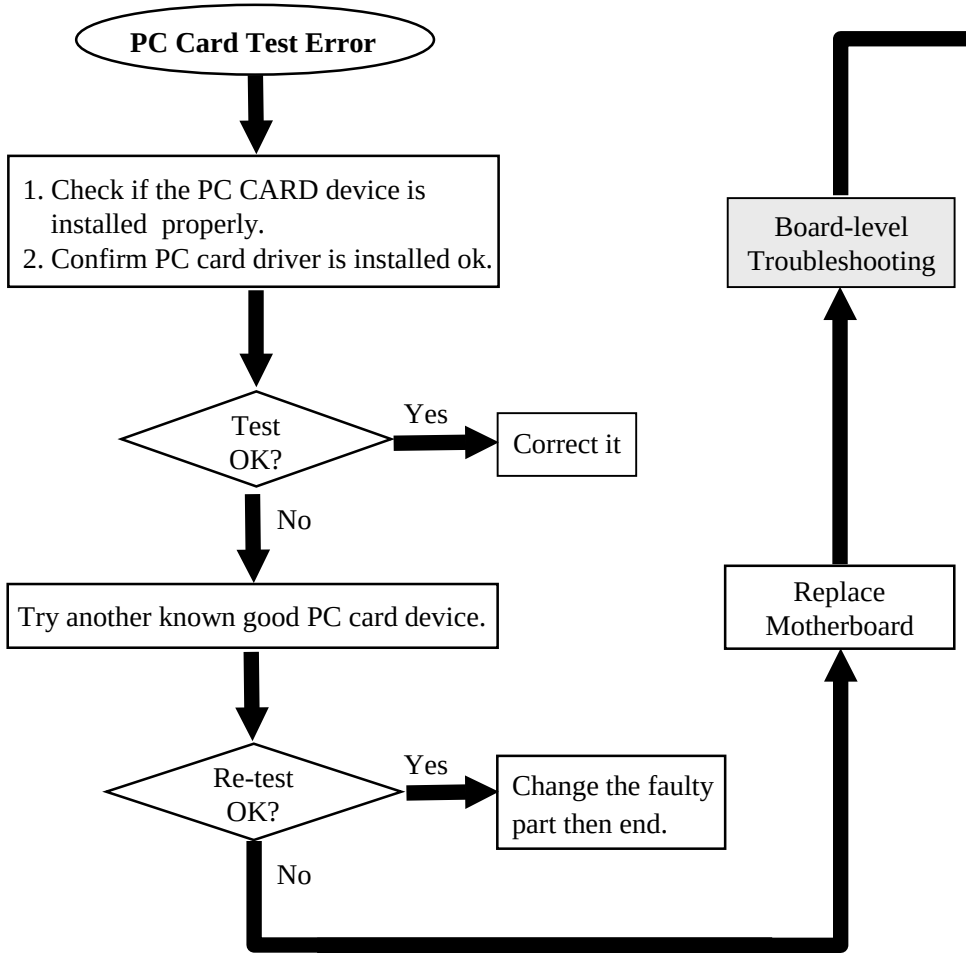
An error occurs when a PC card device is installed.



8.11 PC-Card Socket Failure

Symptom :

An error occurs when a PC card device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U9
U523
J513
R738
R739
R787
R750

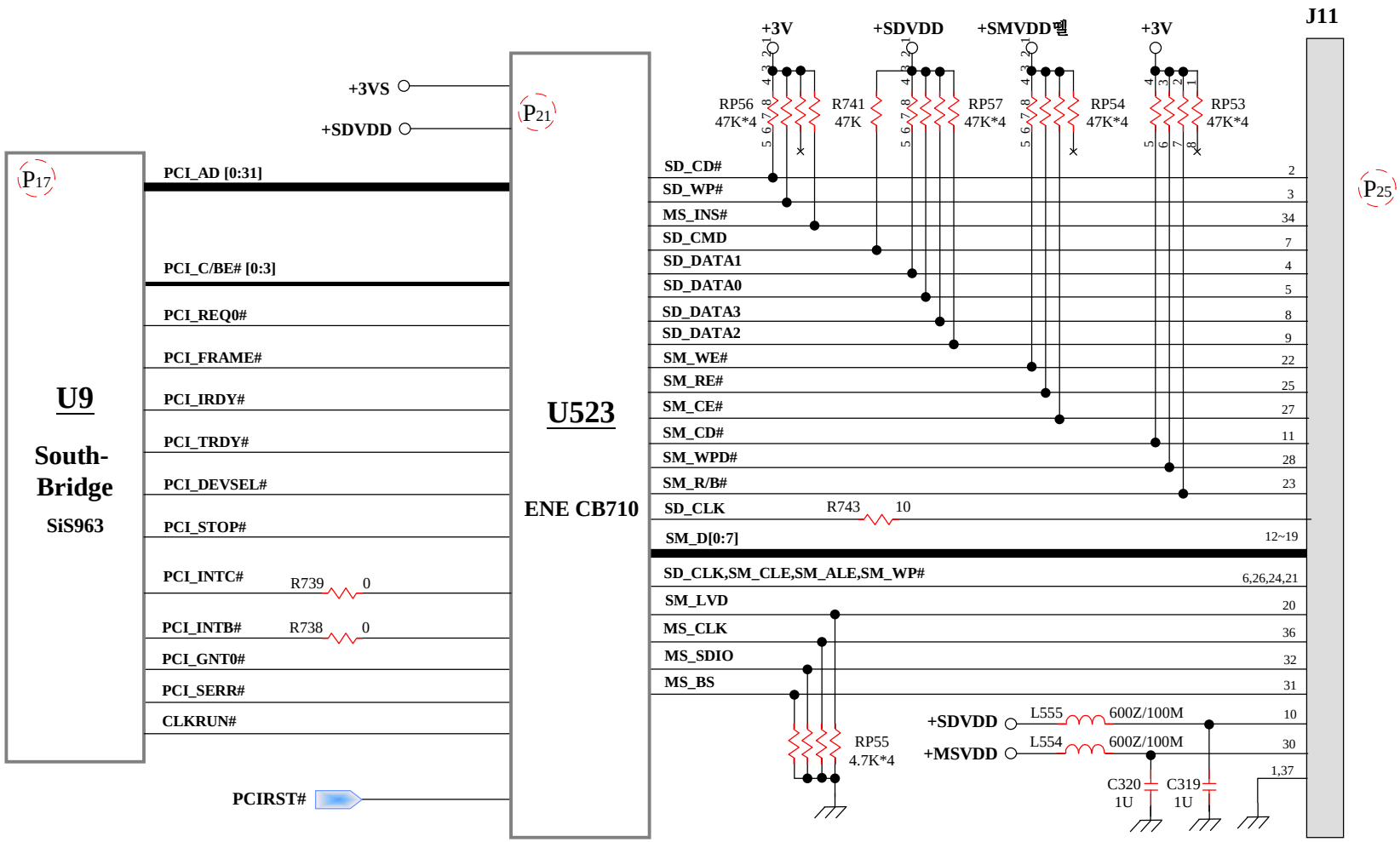
Signals

+3VS
VCCA
SDVDD
CCLKRUN#
CAD[0:31]
CCLK
CCBE#[0:3]
CFRAME#
CPAR
CIRDY#
AUDIO
CTRDY#
CSTSCHG
CVS1#
CVS2#
CINT#
CGINT#
CRST#
CREQ#
CCD1#
CCD2#
CPERR#
CSTOP#
CBLOCK#
R2_A18
R2_D2
R2_D14
CDEVSEL#
PCIRST#

8.12 SD Card Reader Failure

Symptom :

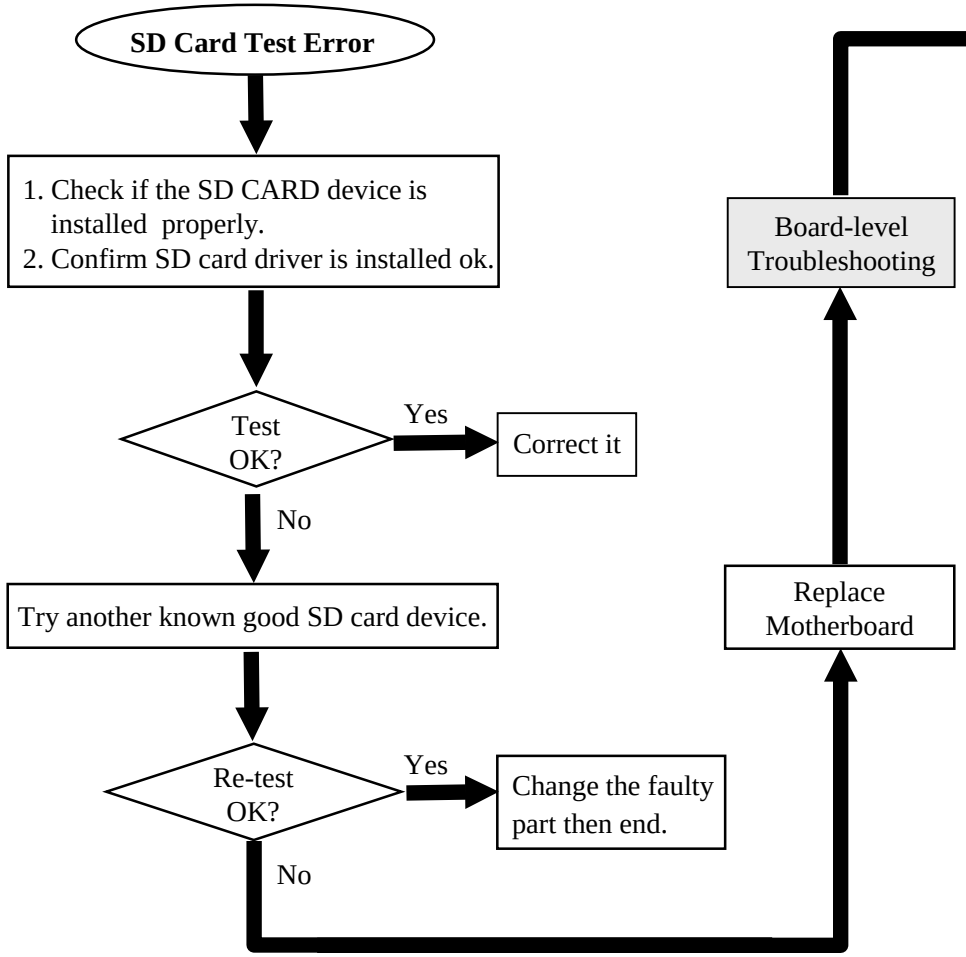
An error occurs when a SD card device is installed.



8.12 SD-Card Reader Failure

Symptom :

An error occurs when a SD card device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**		
U9	PCIRST#	PCI_GNT0#	SM_CD#
U523	+3VS	PCI_SERR#	SM_WPD#
J11	+SDVDD	CLKRUN#	SMR/B
R739	PCI_AD[0:31]	SD_CD#	SD_CLK
R738	PCI_C/BE#[0:3]	SD_WP#	SM_D[0:7]
RP56	PCI_REQ0#	MS_INS#	SM_LVD
R741	PCI_FRAME#	SD_CMD	MS_CLK
RP57	PCI_IRDY#	SD_DATA1	MS_SDI0
RP54	PCI_TRDY#	SD_DATA0	MS_BS
L554	PCI_DEVSEL#	SD_DATA2	SM_CLE
L555	PCI_STOP#	SD_DATA3	SM_ALE
RP55	PCI_INTC#	SM_WE#	SM_WP#
R743	PCI_INTB#	SM_CE#	

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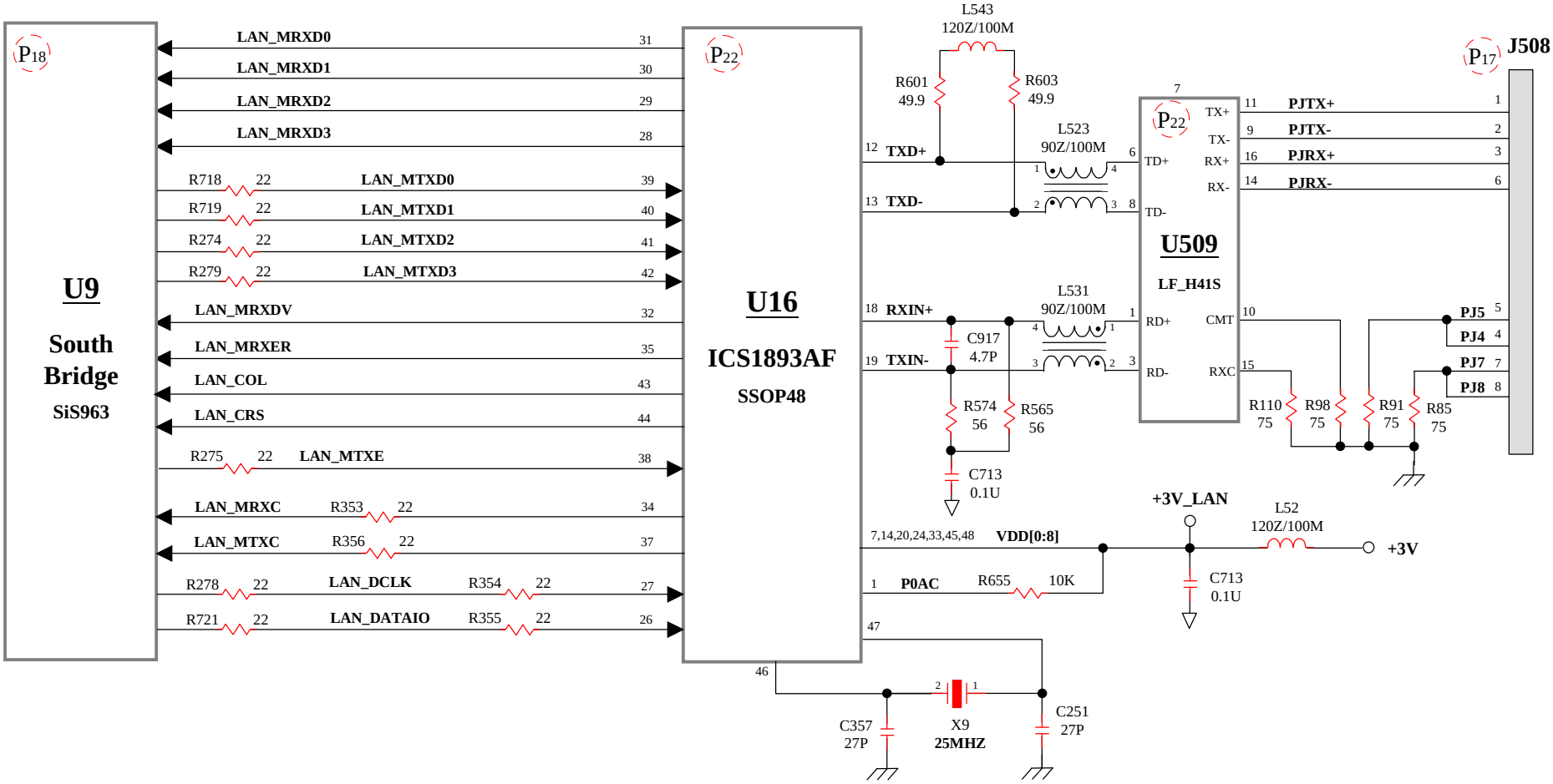
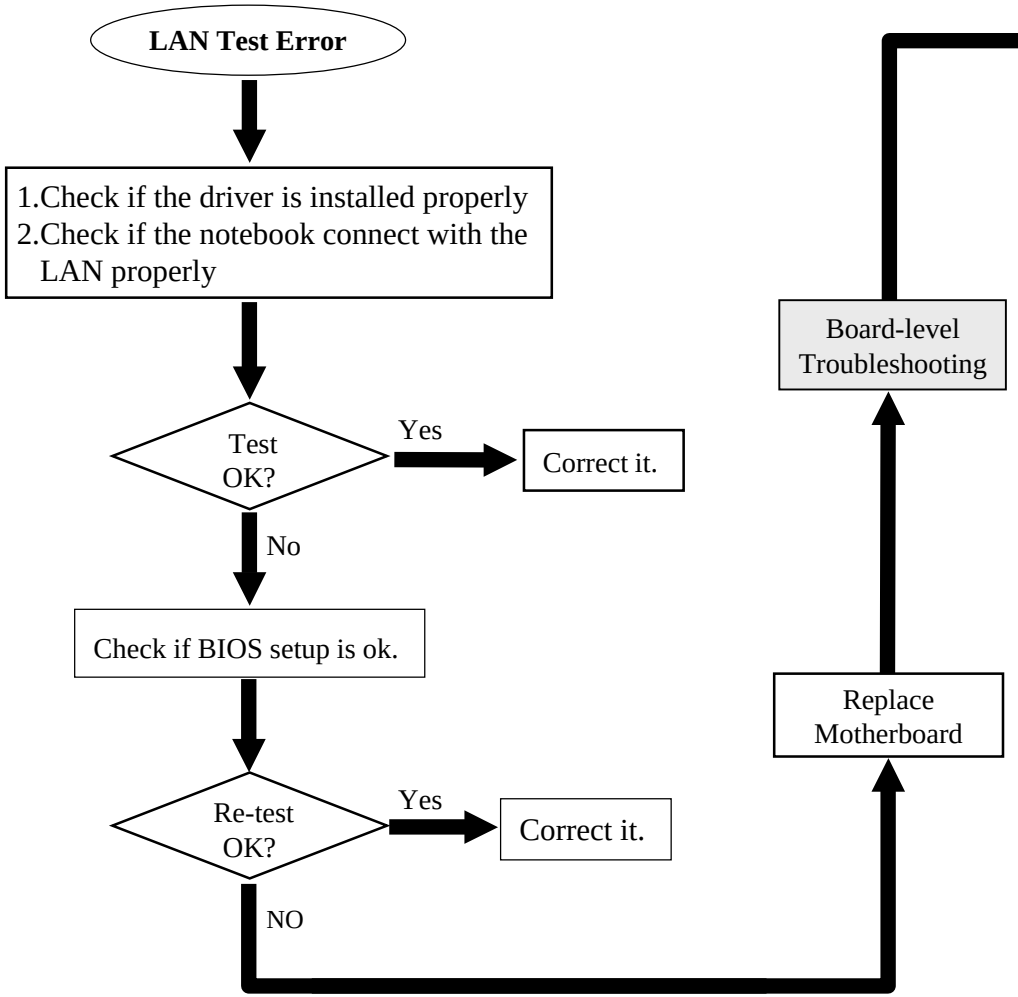
8.13 LAN Test Error

Symptom:
An error occurs when a LAN device is installed.



8.13 LAN Test Error

Symptom:
An error occurs when a LAN device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:		**Signals**	
U9	X9	PJTX+	LAN_MRXD0
U509	C357	PJTX-	LAN_MRXD1
U16	C251	PJRX+	LAN_MRXD2
J508	L543	PJRX-	LAN_MRXD3
R718	L523	PJ4	LAN_MRXDV
R719	L531	PJ5	LAN_MRXER
R274	R601	PJ7	LAN_MRXC
R279	R603	PJ8	LAN_MTXD0
R275	R574	VDD[0:8]	LAN_MTXD1
R353	R655	P0AC	LAN_MTXD2
R356	R565	TXD+	LAN_MTXD3
R278	R110	TXD-	LAN_MTXE
R354	R91	RXIN+	LAN_MTXC
R721	R85	TXIN-	LAN_DCLK
R355	R98	+3V_LAN	LAN_DATAIO
L52			LAN_COL
			LAN_CRS
			+3V

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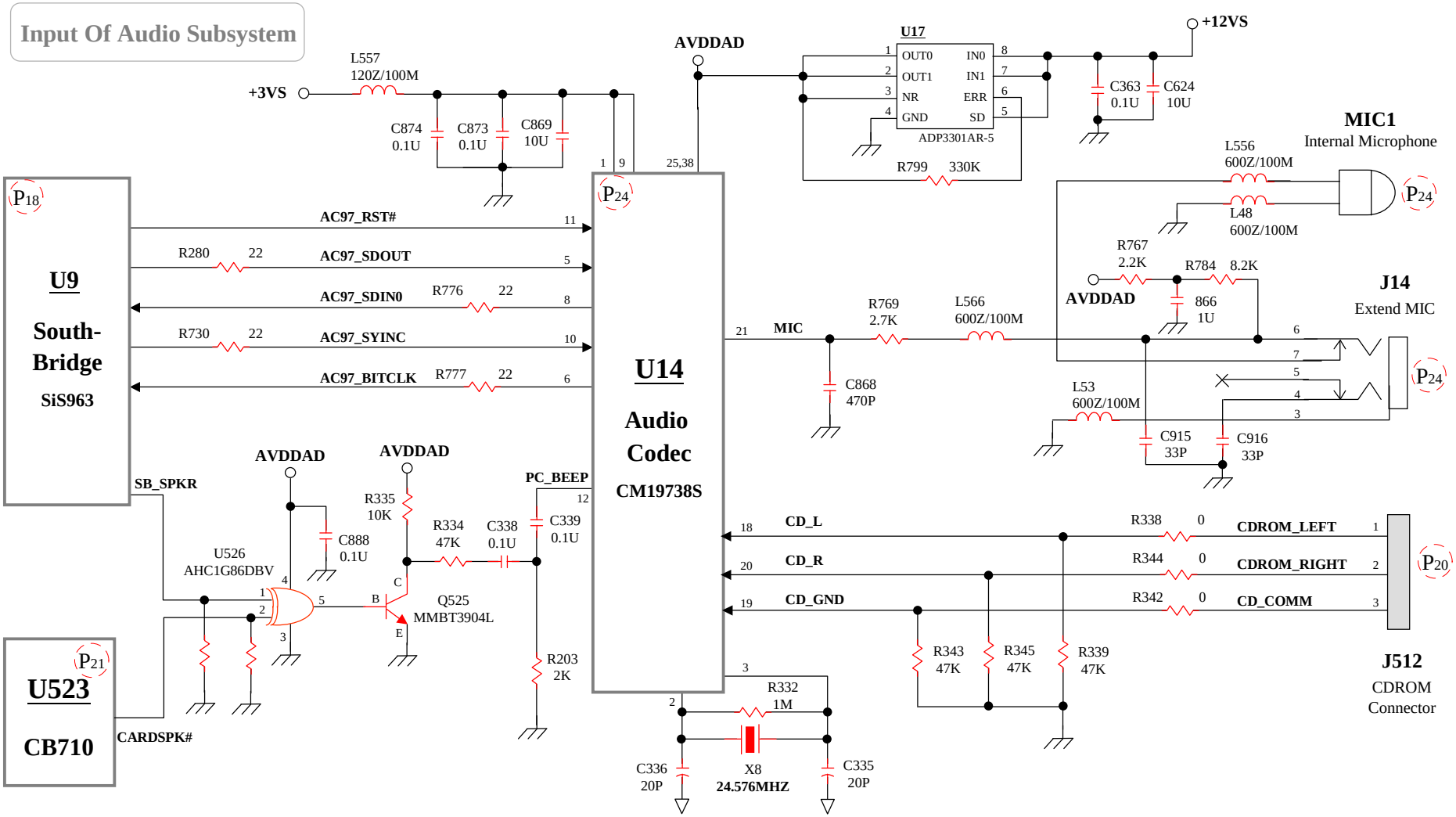
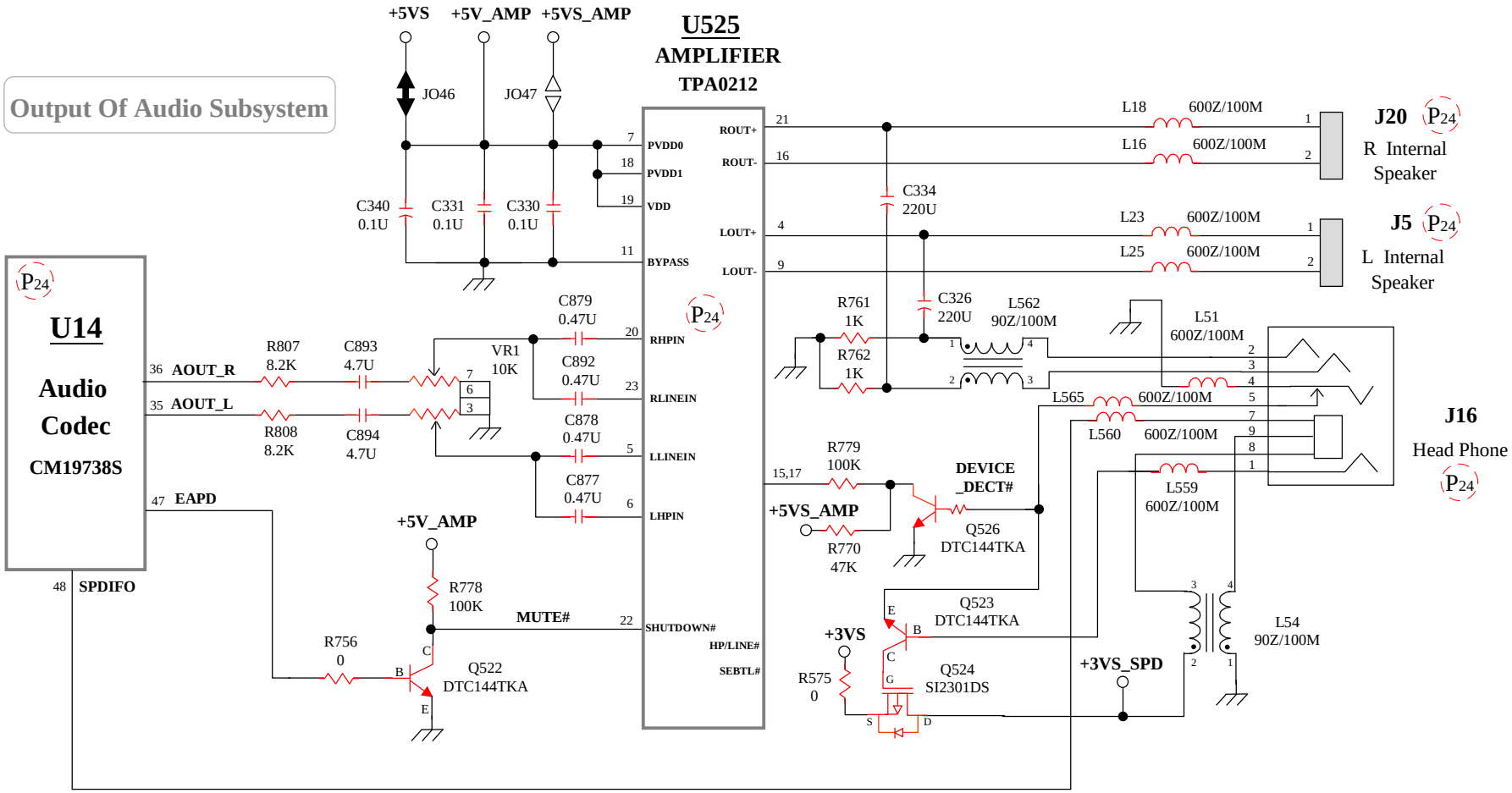
8.14 Audio Failure

Symptom:
No sound from speaker after audio driver is installed.



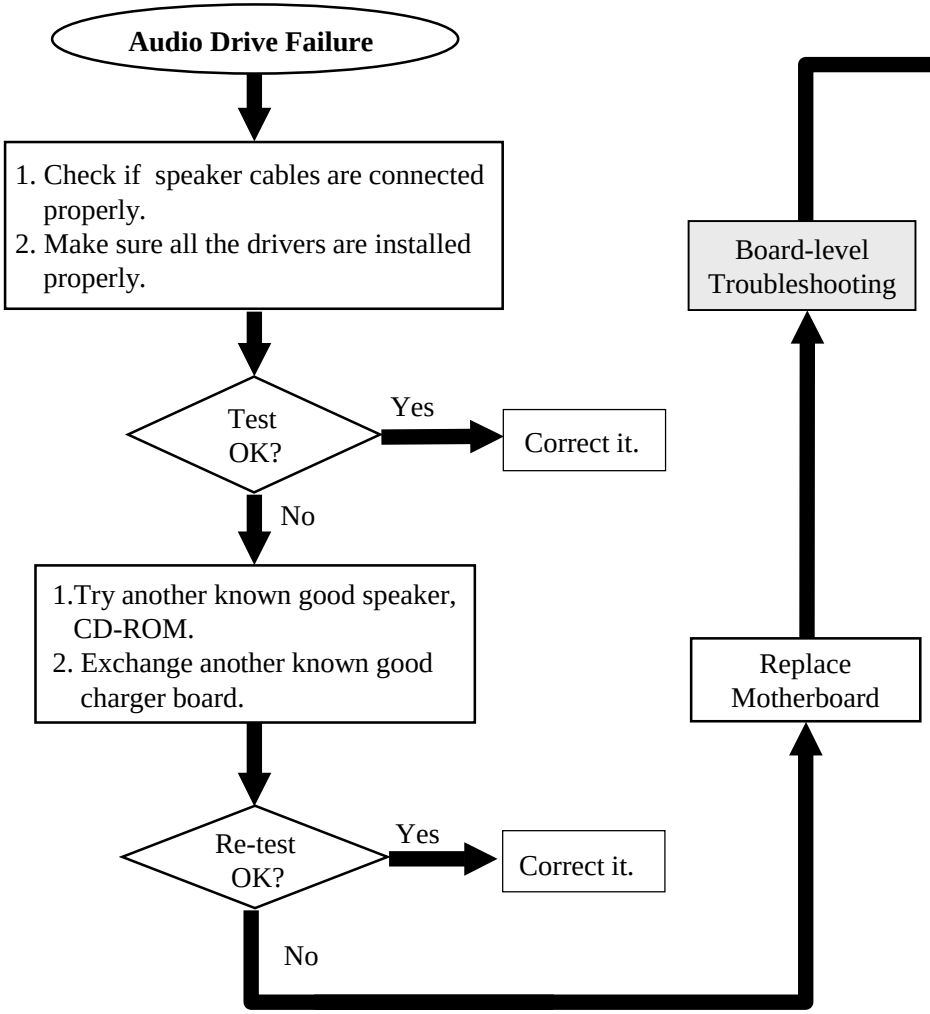
8.14 Audio Failure

Symptom:
No sound from speaker after audio driver is installed.



8.14 Audio Failure

Symptom:
No sound from speaker after audio driver is installed.



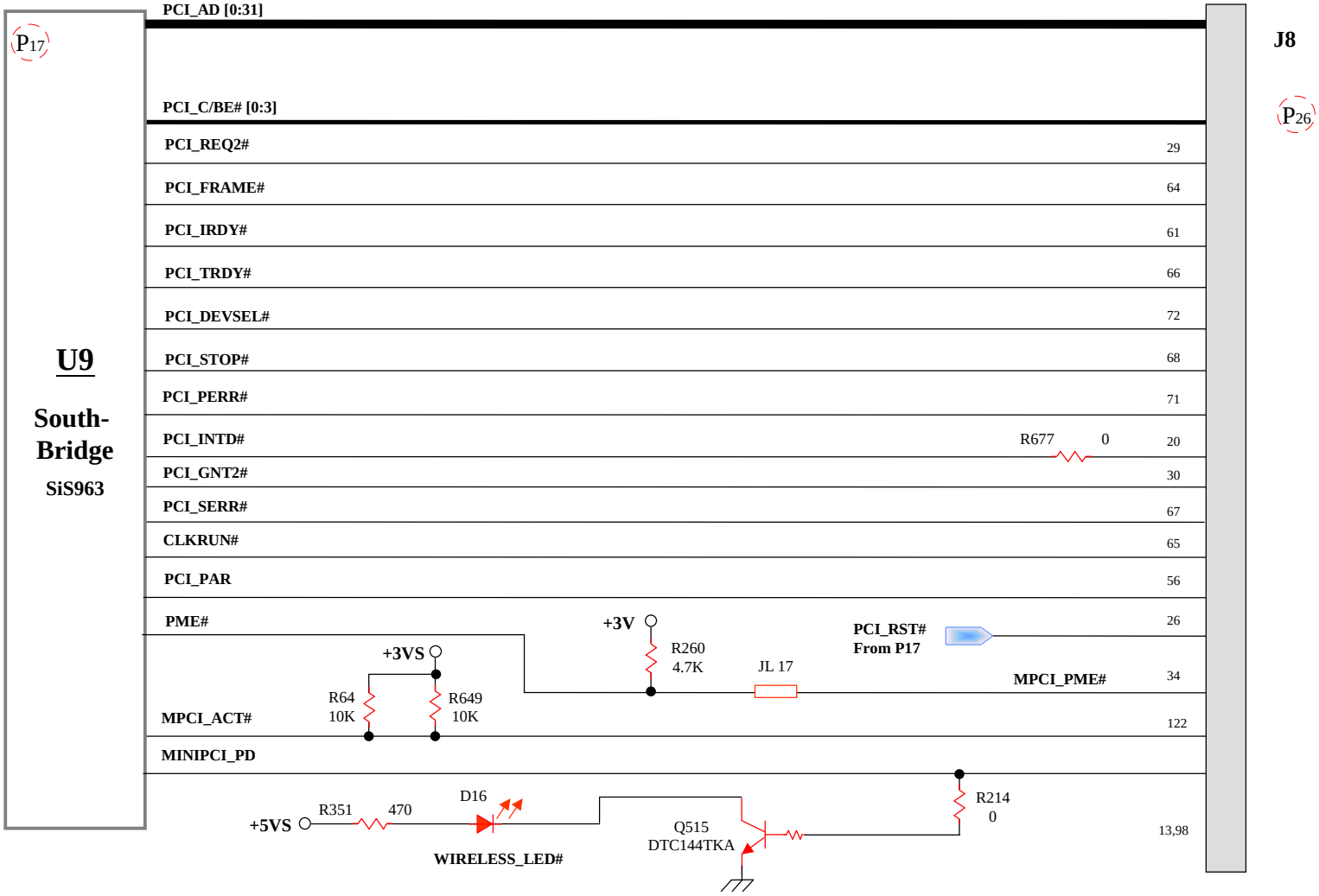
Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:			2. If no sound cause of MIC, check the following parts & signals:		3. If no sound cause of CD-ROM, check the following parts & signals:	
Parts:		**Signals:**	**Parts:**	**Signals:**	**Parts:**	**Signals:**
L23	R893	ROUT+	U9	AVDDAD	J512	CDROM_LEFT
L25	R894	ROUT-	U523	MIC	U9	CDROM_RIGHT
L16	R778	LOUT+	U14	PCBEEP	U523	CDROM_COMM
L18	R756	LOUT-	MIC1	AC97_RST#	U14	CD_R
U14	J20	AOUT_R	J14	AC97_SDOUT	U17	CD_L
U525	J5	AOUT_L	L48	AC97_SDIN0	U526	CD_GND
VR1		EAPD	L556	AC97_SYINC	Q525	
Q522		+5V_AMP	L53	AC97_BITCLK		
R807		+5VS	L566	SB_SPKR		
R808		+5VS_AMP	X8	CARDSPK#		
			U17			

8.15 Mini PCI Test Error

Symptom:

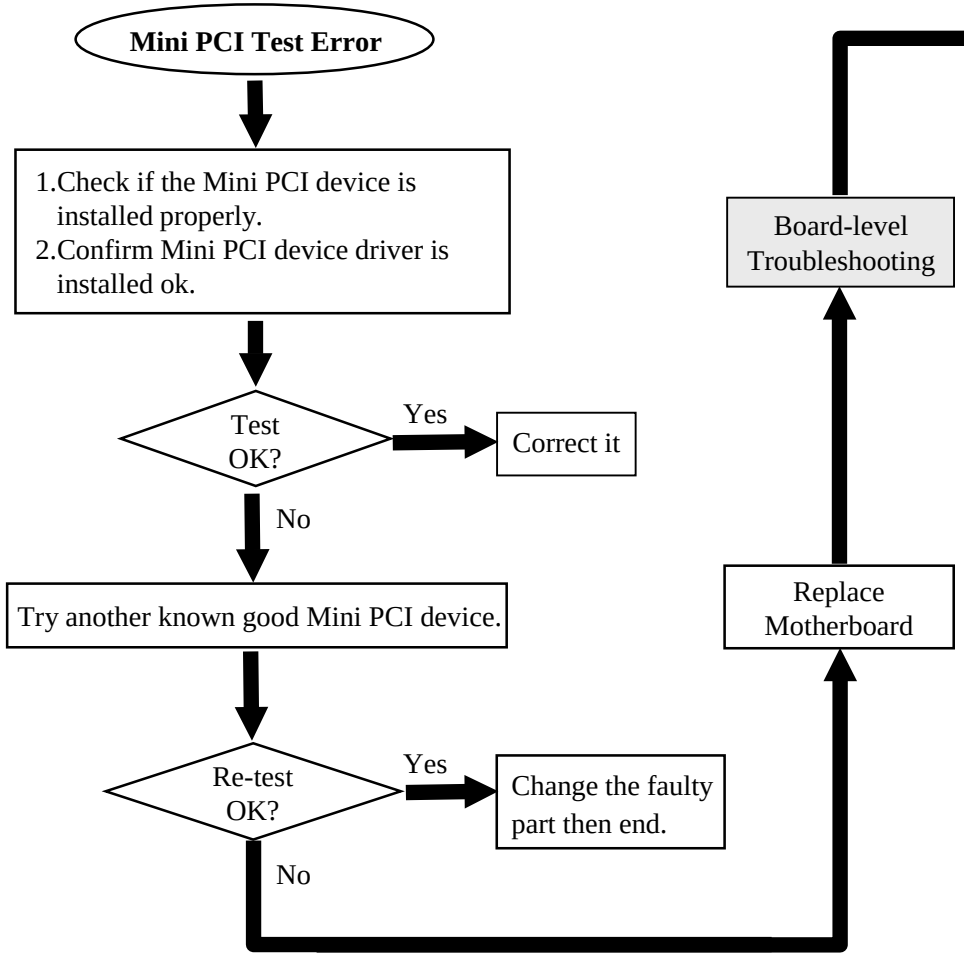
An error message is shown after Mini PCI device is installed or the Mini PCI device does't work.



8.15 Mini PCI Test Error

Symptom:

An error message is shown after Mini PCI device is installed or the Mini PCI device does't work.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U9	PCI_AD[0:31]	PCI_PAR#
J8	PCI_C/BE# [0:3]	PME#
D16	PCI_REQ2#	MPCI_ACT#
Q515	PCI_FRAME#	MINIPCI_PD
R64	PCI_IRDY#	PCI_RST#
R677	PCI_TRDY#	MPCI_PME#
R649	PCI_DEVSEL#	+5VS
R351	PCI_STOP#	+3VS
R260	PCI_PERR#	+3V
R677	PCI_INTD#	
R214	PCI_GNT2#	
	PCI_SERR#	
	CLKRUN#	

9. 8555 Spare Part List-1

Part Number	Description	Location(S)
422675400021	AC ADPT ASSY;19V,7.9A,SPI,150W,S	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
541667830035	AK;01-EN,BOX,3P PW CORD,8555	
541667830031	AK;8555,UTILITY ONLY	
441676230003	BATT ASSY;14.8V,6.6Ah,LI,CASE CL	
441676230004	BATT ASSY;14.8V,6.6Ah,LI,CORE PA	
441676230002	BATT ASSY;14.8V,6600mAH,LI,BL43	
338536010052	BATTERY;LI,3.7V/2.2AH,18650,SANY	
340673500014	BEZEL ASSY;DVDROM,KME,WEASEL	
343675400001	BOSS;STANDOFF,MB,8355	MTG1,MTG2,MTG3
221677040001	BOX,AK,LYNX	
340675400011	BRACKET ASSY;TOUCH-PAD,8355	
342675400013	BRACKET;IO,8355	
342675400006	BRACKET;LCD 15",SPWG,L,8355	
342675400005	BRACKET;LCD 15",SPWG,R,8355	
342675400012	BRACKET;ROM,8355	
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z C	
421673400005	CABLE ASSY;TV-OUT,8640S	
272075103408	CAP ;0.1U CR 50V 10% 0603 X7R S	C15,C16,C35,C37,C38,C39
272005104705	CAP ;1U CR 50V +80-20% 0805 Y5V	C17,C18
272075471409	CAP; 0.0047U CR 50V 10% 0603 X7	C19
272075103706	CAP; 0.1U CR 50V +80-20% 0603 Y	C28,C30,C31,C32,C33,C34
272075223702	CAP; 0.22U CR 50V +80-20% 0603	C29,C40,C41
272075103702	CAP;.01U ,50V,+80-20%,0603,Y5V,S	PC8

Part Number	Description	Location(S)
272075103702	CAP;.01U ,50V,+80-20%,0603,Y5V,S	PC507,PC508
272105103402	CAP;.01U ,CR,25V ,10%,0402,X7R,S	C103,C108,C127,C134,C135,C136
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,S	C7,C8
272072393401	CAP;.039U,CR,16V ,10%,0603,X7R,S	PC533
272105104701	CAP;.1U ,16V,+80-20%,0402,SMT	C162,C19,C229,C232,C233,C234,
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	PC1,PC119,PC12,PC120,PC14,PC
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	PC1,PC4,PC5,PC503,PC504,PC51
272102104401	CAP;.1U ,CR,10V,10%,0402,X5R,SM	C100,C102,C104,C109,C111,C113
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C1,C4,C16,C13
272005104401	CAP;.1U ,CR,50V,10%,0805,X7R,IN	PC525,PC526,PC527
272102334701	CAP;.33U ,CR,10V ,+80-20%,0402,Y	C886
272002474401	CAP;.47U ,CR,16V ,10%,0805,X7R,S	C857,C858,C859,C870,C877,C878
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TU	C131,C69,C70
272105102408	CAP;1000P,CR,50V,10%,0402,X7R,SM	C248,C25,C26,C38,C49,C54,C57,
272105101402	CAP;100P ,50V ,+ -10%,0402,NPO,S	C18,C502,C503,C504,C864,C865,
272105101401	CAP;100P ,50V ,5%,0402,COG,SMT	PC105,PC538,PC570,PC89,PC96
272075101302	CAP;100P ,CR,50V,5%,0603,NPO,SMT	C11
272010101302	CAP;100P,2KV,5%,1206,NPO,SMT,onl	C15
272010101301	CAP;100P,2KV,5%,1206,NPO,SMT,onl	
272105100303	CAP;10P ,CR,50V ,5%,0402,NPO,SM	C173,C298,C302,C33,C34,C35,C7
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C501,PC11,PC539,PC550,PC555
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	PC509,PC511,PC512
272011106407	CAP;10U,10V,+/-10%,1206,X5R,SMT,	PC117,PC85,PC9
272011106408	CAP;10U,16V,+/-10%,1206,X5R,SMT,	C23,C231,C24,C252,C295,C309,C
272043106401	CAP;10U,25V,+-10%,1812,X5R,SMT,T	PC502,PC506,PC510,PC518,PC51

9. 8555 Spare Part List-2

Part Number	Description	Location(S)
272043106403	CAP;10U,25V,+-10%,1812,X5R,SMT,T	
272993106001	CAP;10U,25V,2.2mm,X5R,KYOCERA,SM	PC511,PC512,PC513,PC517,PC51
272023106002	CAP;10U,25V,M,1210,T2.8MM,X5R,SM	PC126,PC16,PC572,PC70,PC73,P
272011106404	CAP;10U,6.3V,10%,1206,X7R,SMT	C105,C106,C126,C137,C163,C164
272075120301	CAP;12P ,CR,50V ,5% ,0603,NPO,S	C313,C318,C328,C342
272075152401	CAP;1500P,CR,50V,10%,0603,X7R,SM	PC569,PC91
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	C890
272433156502	CAP;15U ,TQC,25V,20%,H=1.9 ,7343	PC36,PC37,PC38,PC39,PC40,PC4
272433156502	CAP;15U ,TQC,25V,20%,H=1.9 ,7343	PC521
272075181301	CAP;180P ,50V ,5% ,0603,NPO,SMT	PC97
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C154,C155,C308,C314
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	PC50,PC507,PC51,PC532,PC534,
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	PC505,PC514
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C9
272001105402	CAP;1U ,CR,10V,10%,0805,X5R,SM	C6
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC3
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC7,PC8
272102105701	CAP;1U ,CR,6.3V ,80-20%,0402,Y	C114,C116,C118,C119,C124,C125
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5	PC46,PC47,PC48
272001225401	CAP;2.2U ,CR,10V ,10%,0805,X7R,S	C5
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C301,PC65
272105200401	CAP;20P ,50V,+-10%,0402,SMT	C289,C291,C335,C336
272105222501	CAP;2200P,50V ,+/-20%,0402,X7R,S	C112,C632
272105222301	CAP;220P ,50V ,5% ,0402,NPO,SMT	C156,C871,C89,C91,C99
272075221302	CAP;220P ,50V ,5% ,0603,NPO,SMT	C1,C10,C11,C12,C13,C14,C15,C16

Part Number	Description	Location(S)
272075221401	CAP;220P ,CR,50V ,10%,0603,X7R,S	PC531,PC540
272431227001	CAP;220U, 2.5V,TPE, 7343,18MR	PC10,PC501,PC557,PC558,PC68,
272421225501	CAP;220U,TPE,4V,20%,7343,SMT	PC543,PC546,PC549,PC552
272075220303	CAP;22P ,50V ,5% ,0603,NPO,SMT	C256,C257
272011226401	CAP;22U,6.3V,+-20%,1206,X5R,SMT	C130,C133,C174,C196,C202,C211
272105271403	CAP;270P ,50V,+-10%,0402,X7R,SMT	C150,C20,C21,C22,C856,C884
272105270303	CAP;27P ,50V ,5%,0402,COG,SMT	C251,C357
272075331301	CAP;330P ,CR,50V,5% ,0603,NPO,SM	C12
272431337512	CAP;330U,2V,20%,7343,9mOHM,H2.8m	
272431337511	CAP;330U,2V,20%,7343,ESR7m,H2.8m	PC27,PC30,PC31,PC32,PC33,PC3
272421336501	CAP;33U ,TT,6.3V,20%,3528,SMT	C535,C543
272075479301	CAP;4.7P,50V,5%,0603,NPO,SMT	C917
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C358,C893,C894
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C786,C789,C839,C844
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C14
272105471403	CAP;470P ,50V,10%,0402,X7R,SMT	C185,C199,C215,C216,C868
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	C36
272431476502	CAP;47U ,6.3V,20%,SP-CAP,7343,S	C2
272431476504	CAP;47U,6.3V,20%,AO-CAP,7343,SMT	
272431476503	CAP;47U,6.3V,20%,PC-CON,7343,SMT	
272030050302	CAP;5P,3KV,5%,1808,NPO,SMT,only	C17
272030050301	CAP;5P,3KV,5%,1808,NPO,SMT,only	
272075680302	CAP;68P ,50V ,5% ,0603,NPO,SMT	C307
221675450007	CARD BOARD;W/AK BOX,FRAME,PALLET	
221675450008	CARD BOARD;W/AK BOX,T/B,PALLET,8	

9. 8555 Spare Part List-3

Part Number	Description	Location(S)
221600020252	CARTON;BATTERY,CAIMAN,PWR	
221675420004	CARTON;W/AK BOX,N-B,8355	
431678330001	CASE KIT;8555H ID1	
335152000026	CFM-BAT;FUSE,THERMAL,NEC,SF91E	
273000500095	CHOCK COIL;0.5UH.1.0mOHM,25%,30A	PL502,PL503,PL504
273000500111	CHOCK COIL;3UH,14mOHM,7.5A,10039	PL6,PL7
273000500096	CHOCK COIL;4.7UH.20mOHM,25%,4.5A	PL501
273000500115	CHOKE COIL;400uH MIN,120mΩ MAX;	L521
273000500084	CHOKE COIL;400UH(REF),D.2*1,10.5	
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L10,L13,L15,L523,L531,L54,L56
273000150314	CHOKE COIL;90OHM/100MHZ,20%,2012	
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/P	
331000008038	CON;BAT,8P,2.5MM,SUYIN	PJ502
331000004036	CON;BATTERY,0402A120,4P,R/A,8500	PJ501
331000007015	CON;BATTERY,FM,7P,R/A,8175,PRC	CON2
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J502
331720025005	CON;D,FM,25P,2.775,R/A	J503
291000025027	CON;FM,0.8MM,25P*2,R/A,SMT,Allt	J512
291000151201	CON;FPC/FFC,12P,0.5MM,R/A,SMT	J9
291000152604	CON;FPC/FFC,26P,1MM,R/A,ELCO,SMT	J29
291000144004	CON;HDR,20P*2,1.0MM,H=4.6,ST,SMT	J2
291000141002	CON;HDR,5P*2,1.0MM,H=4.6,ST,SMT,	J13
291000141002	CON;HDR,5P*2,1.0MM,H=4.6,ST,SMT,	J501
291000022610	CON;HDR,FM,13P*2, 2.00mm,ST,SMT,	PJ503
291000023002	CON;HDR,FM,15P*2,0.8MM.H4.4,R/A,	J12

Part Number	Description	Location(S)
291000014409	CON;HDR,FM,22P*2,2.0MM,SMT,SPEED	J511
291000021104	CON;HDR,MA,11P*1,1.25,R/A,3811Y-	J1
291000021101	CON;HDR,MA,11P*1,1.25,R/A,DF13-1	
291000021103	CON;HDR,MA,11P,1.25MM,R/A,SMT,DF	
291000011201	CON;HDR,MA,12P*1,1.25MM,ST,SMT	J3
291000022611	CON;HDR,MA,13P*2, 2.00mm,ST,H=4.	PJ1
291000010201	CON;HDR,MA,2P*1,1.25MM,ST,SMT	J10,J20,J4,J5
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	J2
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	
291000010301	CON;HDR,MA,3P*1,1.25MM,ST,SMT	J1,J509,J514
331000004009	CON;IEEE1394,MA,4P*1,0.8MM,R/A	J15
291000253701	CON;MEMORY CARD,37P,SD,SM,SSFDC,	J11
331000007018	CON;MINI DIN,7P,R/A,W/GROUND,ALL	J501
291000616801	CON;PCMCIA CARD,68P,TAI-SOL,WEAS	J513
291000811001	CON;PHONE JACK,10P,R/A,RJ45,RJ11	J508
331840010008	CON;STEREO JACK,10P,W/SPDIF,R/A,	J16
331840005013	CON;STEREO JACK,5P,R/A,28MF60-07	J14
331000004029	CON;USB,MA,R/A,4P*1,2551A-04G5T-	J504,J505,J506,J507
346675400029	CONDUCTIVE TAPE;DC IN,MB,8355	
345678300022	CONDUCTIVE TAPE;LCD PANEL,8555	
345678300011	CONDUCTIVE TAPE;T/P BRAKCET,UP,8	
225675400001	CONDUCTIVE TAPE;TOP ASSY,DDR,RIG	
345678300012	CONDUCTIVE TAPE;TP BRAKCET,LEFT,	
345678300013	CONDUCTIVE TAPE;TP BRAKCET,RIGHT	
345678300013	CONDUCTIVE TAPE;TP BRAKCET,RIGHT	

9. 8555 Spare Part List-4

Part Number	Description	Location(S)
441676230032	CONTACT PLATE ASSY;FUSE,S-TUBE,B	
441676230031	CONTACT PLATE ASSY;PTC,S-TUBE,BL	
441676230035	CONTACT PLATE ASSY;W5L45T0.13,S-	
441676230034	CONTACT PLATE ASSY;W5L9T0.13,S-T	
441676230033	CONTACT PLATE ASSY;W7L68.4T0.13,	
342668200003	CONTACT PLATE;2,W4L20T0.15	
342503400007	CONTACT PLATE;W5L45T0.13 ,1/3T,7	
342503400004	CONTACT PLATE;W5L45T0.13,7170LI,	
342503400004	CONTACT PLATE;W5L45T0.13,7170LI,	
342503400002	CONTACT PLATE;W5L9T0.13,7170LI,P	
342503400003	CONTACT PLATE;W7L7T0.13,7170LI,P	
342676200001	CONTACT PLATED; W7L104.8T0.13; P	
342676200002	CONTACT PLATED; W7L50.2T0.13; PW	
342674800002	CONTACT PLATED;W5L31T0.13	
342674800003	CONTACT PLATED;W7L68.4T0.13	
340675400014	COVER ASSY;CPU,8355	
340675400007	COVER ASSY;LCD 15",8355	
340675400010	COVER ASSY;SPEAKER,K/B,8355	
340678300002	COVER ASSY;TOP,8555	
344675400021	COVER;BATTERY,8355	
344675400024	COVER;HDD,8355	
344675400016	COVER;HINGE,8355	
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP1,CP2
323767720004	DDR SODIMM MODULE;256MB,77.10634	
291000612005	DIMM SOCKET;DDR 200P,0.6MM,H4,SM	

Part Number	Description	Location(S)
291000612022	DIMM SOCKET;DDR NOR,200P,0.6MM,H	
291000612014	DIMM SOCKET;DDR REVERSE,200P,0.6	J7
291000612023	DIMM SOCKET;DDR RVS,200P,0.6MM,H	
291000612013	DIMM SOCKET;DDR STANDARD,200P,0.	J6
291000612004	DIMM SOCKET;DDR,200P,0.6MM,H4,SM	
288111544001	DIODE; 1SR-154-400 400V 1.0A	D4
288110355001	DIODE;1SS355,80V,100mA,SOD-23,SM	D3
288100541002	DIODE;BAT54ALT1,COM. ANODE,SOT-2	PD1,PD13,PD505
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D10,PD3,PD4
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D1
288100056003	DIODE;BAW56,70V,215mA,SOT-23	D508
288100056003	DIODE;BAW56,70V,215mA,SOT-23	PD3
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD11,PD506
288100112003	DIODE;EC11FS2-TE12L,SCHOTTKY,200	D501,PD507
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD12,PD5,PD501,PD502,PD503,I
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD1,PD2,PD502
288100805001	DIODE;ESD0805A,1CH,15KV,0805,2P	D19,D20,D21,D22,D512,D513,D5
288100551001	DIODE;RB551V-30,SCHOTTKY,.36V,UM	D507
288200717001	DIODE;RB717F,SCHOTTKY,40V,SOT323	SD2
288100751001	DIODE;RB751V-40,40V,200mA,SOD-32	D9
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D11,D17,D18,D5,D502,D504,D50
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD2
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	PD504
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	ZD3,ZD4
344672300025	DUMMY CARD;PCMCIA,MANGUSTA	

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Part Number	Description	Location(S)
523467830004	DVD ASSY;KME,SR-8177-CPK2,8555	
523481614001	DVD-ROM DRIVE;SR-8177-CPK1	
272602227502	EC;220U ,16V,M,D6.3*7.7,-55+105'	C505,C506,C520,C548
272601227507	EC;220U ,6.3V,M,D6.3*5.8,-55+105	C326,C334
312273306154	EC;330U ,4V ,+-20%,100*5,SP.OS-	PC103
312276806158	EC;680U,6.3V,20%,RA,10*10.5,105	PC580
227675400004	END CAP;W/AK BOX,8355	
227675400003	EPE PAD;K/B,8355	
481678300004	F/W ASSY;KBD CTRL,8555H	U10
481678300003	F/W ASSY;SYS/VGA BIOS,8555H	U8
340675400029	FAN ASSY;IO,8355	
340678300018	FAN ASSY;IO,YS,8555	
273000610025	FERRITE ARRAY;120OHM/100MHZ,ONLY	
273000610025	FERRITE ARRAY;120OHM/100MHZ,ONLY	FA1,FA501
273000610013	FERRITE ARRAY;120OHM100MHZ,3216,	RP501,RP502,RP503,RP504
273000150307	FERRITE BEAD;120 OHM/100MHZ,3A,0	
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,	L26,L27,L28,L3,L33,L36,L37,L38
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	
273000130009	FERRITE CHIP;120OHM/100MHZ,1608,	
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L11,L12,L20,L30,L43,L45,L501,L
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	PL2,PL3,PL501,PL502
273000130010	FERRITE CHIP;130OHM/100MHZ,1608,	R777
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	
273000130015	FERRITE CHIP;220OHM/100MHZ,1608,	L6,L7,L8
273000150009	FERRITE CHIP;30OHM/100MHZ,2012,3	L34,L35,L540

Part Number	Description	Location(S)
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L1,L16,L18,L23,L25,L31,L48,L50
422675400001	FFC ASSY;TOUCH-PAD,8355	
341669900011	FINGER;EMI GROUND SMD FINGER,H=3	TP538,TP539
288001001001	FIR,GP2W1001YP,GDE VIEW,10P,SMT,	U15
245600010007	FLOW CARD;M/B,WHITE	
295000010044	FUSE;1.1A/6V,POLY SWITCH,1210,SM	F2,F501,F505
295000010057	FUSE;228R,139C',5A/250V,SMT,PRC	F2
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF1,PF501
295000010140	FUSE;FAST,2A,63VDC,1206,SMT,0433	
295000010134	FUSE;FAST,2A,63VDC,1206,SMT,PRC	F1
335152000062	FUSE;LR4-730,POLY SWITCH,PRC	
346678300025	GASKET;AL-FOIL,MB,8555	
345678300001	GASKET;CARDREADER,MB,8555	
345678300002	GASKET;ROM,MB,8555	
345678300005	GASKET;S-TERMINAL ,MB,8555	
345678300010	GASKET;TUNER,MB,8555	
523467830024	HDD ASSY;40G,HGST IC25N040ATMR04	
523405320072	HDD DRIVE,40GB,2.5",IC25N040ATMR	
451678300071	HDD ME KIT;8555	
340678300012	HEATSINK ASSY;CPU,NORTHWOOD,FORC	
343678300001	HEATSINK;MOS,8555,MPT	
343675400003	HEATSINK;NORTH BRIDGE,MPT,8355	
340675400006	HINGE;L,15",8355	
340675400005	HINGE;R,15",8355	

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Part Number	Description	Location(S)
344674300038	HOLDER;PCMCIA,TAI-SOL,P2P2601-22	
340678300013	HOUSING ASSY;HOUSING,8555	
340675400003	HOUSING ASSY;LCD 15",8355	
451678300051	HOUSING KIT;8555 ID1	
344675400022	HOUSING;BATTERY,8355	
331650047804	IC SOCKET;BGA-PGA478B-SKT,MOLEX,	U508
286304377001	IC; MAX4377F,I-SENSEAMP ,MSOP8,S	PU506
282574108002	IC;74AHC1G08,SINGLE AND GATE,SOT	U507
282574373004	IC;74AHC373,OCT D-TRAN,TSSOP,20P	U521
282574186002	IC;74AHCT1G86,SINGLE,XOR,SOT23,S	U526
282074338402	IC;74CBTD3384,10 BIT BUS SW,TSOP	U12
286303301001	IC;ADP3301AR-5,.8%,REG.,SO,8P	U17
286308800006	IC;AME8800AEEV,VOL REG.,SOT23-5,	PU10
286301117020	IC;APL1117,1A,LDO,ADJ,SOT223,3PI	PU15,PU17
284500010003	IC;ATI MOBILITY M10-P,AGP,BGA 70	U6
286300710001	IC;CB710,PCI/CARDBUS,LQFP,208P,S	U523
284509738002	IC;CMI9738-S,AC97 CODEC,LQFP,48P	U14
286302211006	IC;CP2211,POWER DISTRI SW,REV.C1	U522
324180786553	IC;CPU,P4 DESKTOP,CELERON,2.4G F	
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SM	IC6
283467540002	IC;EEPROM,M93C46-WMN6T,64*16 BIT	U520
283700320001	IC;EM6AA320BI-3.6M,DDR SDRAM,8MX	U510,U512,U513,U514
286301655002	IC;FAN1655,REGULATOR,ETSSOP-16	PU507
286305234001	IC;FAN5234,PWM,QSOP,16P	PU2
283460000003	IC;FLASH,512K*8-70,PLCC32,EN29F0	

Part Number	Description	Location(S)
283410310002	IC;FLASH,512K*8-90,PLCC32,W29C04	
284500803002	IC;FW803,IEEE1394 PHY,LQFP64P,3P	U13
286300690003	IC;G690E,RESET CIRCUIT,4.38V,SOT	U11
284583437003	IC;H8/F3437S,KBD CTRL,TQFP,100P,	
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	PU26
284501893002	IC;ICS1893AF,LAN PHY,SMT,SSOP48	U16
284593772001	IC;ICS93772,DDR ZERO DELAY CLOCK	U516
284595201101	IC;ICS952011,CLOCK GEN,TSSOP,48P	U7
286306207001	IC;ISL6207CB,PWM DRIVER,SO8,SMT	PU4,PU5,PU6
286306247001	IC;ISL6247,PWM CONTROLLER,40-QFN	PU503
284500086001	IC;LM86,TEMPERATURE MTR,SO8	U4,U511
286100358001	IC;LMV358M,DUAL AMP.,LOW VOLT.,S	PU7
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU9
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	PU8
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QF	PU16,PU23
286301772001	IC;MAX1772,PWM,QSOP,28P	PU502
286305258001	IC;MIC 5258-1.2BM5,LV12,LDO REG,	U503
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PR	IC7
286300965001	IC;OZ965R,CCFL CTRL,TSSOP16,O2	U1
284502779001	IC;P2779A,EMI REDUCTION,SO8	U5
284587393002	IC;PC87393F,TQFP,100P	U519
286309181002	IC;RT9181, 150mA LDO with POG,SO	
284509181001	IC;RT9181,150MA CMOS LDO,1.2V,SO	
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U2,U501
286387506001	IC;S-875061EUP VOLT DETECTOR S	IC5

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Part Number	Description	Location(S)
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ502,PQ509
284500648004	IC;SIS648FX,N.B.,BGA 830P	U506
284500963003	IC;SIS963,S.B.,BGA 371P	U9
286100212001	IC;TPA0212,AMPLIFIER,TSSOP,24P,S	U525
273000990012	INDUCTOR;10UH,CDRH127,SUMIDA,SMT	PL512
273000990012	INDUCTOR;10UH,CDRH127,SUMIDA,SMT	PL1
273000990031	INDUCTOR;10UH,CDRH127B,SUMIDA,SM	PT501
273000990175	INDUCTOR;3.3UH,20mOHM,8A,10043,S	
273000150106	INDUCTOR;4.7UH,10%,2012,30mA,SMT	L515,L518
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346678300001	INSULATOR;AL-FOIL,M/B,8555	
346678300026	INSULATOR;ASSY,6CELL,SINGLE FACE	
346503100301	INSULATOR;BATT ASSY,6CELLS,7521C	
346503400502	INSULATOR;BATT ASSY,L22R9.2,8175	
346503200006	INSULATOR;BATT ASSY,ONE ROUND,GR	
346675400026	INSULATOR;BATT ASSY,POLY,W30L53,	
346503400503	INSULATOR;BATT ASSY,W7L13,8175	
346668300024	INSULATOR;DIMM P/N MB TOP,HOPE	
346503200201	INSULATOR;FOR 2CELL/2ADHESIVE,WE	
346503200002	INSULATOR;FOR 4 CELLS,GRAMPUS	
346669900004	INSULATOR;INVERTER,7170	
346675400023	INSULATOR;M/B,MDC,8355	
346675400017	INSULATOR;MINI PCI,8355	
346676200003	INSULATOR;PC GE FR-1,t=0.25mm; P	FOR CELL AND NICKLE
346678300002	INSULATOR;ROM,8555	

Part Number	Description	Location(S)
346678300014	INSULATOR;TUNER,MB,8555	
531017240150	KBD;88,US,3000170351,ZIPPY,8555	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000439	LABEL;25*6,HI-TEMP,COMMON	
242600000439	LABEL;25*6,HI-TEMP,COMMON	
242600000385	LABEL;27*10,LAN ID BAR CODE	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242679900005	LABEL;BAR CODE,(25*10MM)*12pcs,8	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242678300002	LABEL;BATT 14.8V/6.6AH,LI,SANYO,	FOR COVER
242600000433	LABEL;BLANK,11*5MM,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242600000001	LABEL;PAL,20*5MM,COMMON	
441678300035	LCD ASSY;15",XGA,QDI,8555 ID1	
451678300035	LCD ME KIT;15",XGA,QDI,8555 ID1	

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Part Number	Description	Location(S)
413000020396	LCD;QD15XL06,TFT,15.0",XGA,QDI	
294011200155	LED;BLUE,H0.8,SF0603-B70140-30,S	D15,D16
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190	LED1,LED2,LED3,LED4
294011200034	LED;GREEN,H.8,0603,19-21VGC/TR,S	
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D1,D10,D3,D5,D7
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SR	LED5,LED6
416267833005	LT PF;15",XGA,QDI,8555H ID1	
561567830001	MANUAL KIT;EN,8555,N-B	
561567830101	MANUAL;USER'S,EN,8555,N-B	
339115000052	MICROPHONE;OF-D50P40,-40+-2dB,2.	MIC1
291000611247	MINIPCI SOCKET;124P,0.8MM,H=4.0,	J8
344675400015	NAME-PLATE;SPEAKER COVER,8355	
451678300091	ODD ME KIT;8555	
461675400006	PACKING KIT;N-B,8355	
224673130001	PALLET;COMPLEX,1300x1100x126,806	
221600050218	PARTITION;BATTERY,MARLIN,CAIMAN,	
221675350014	PARTITION;HDD ME KIT,8080	
221600050219	PARTITION;TOP/BTM,BATTERY,MARLIN	
221675450009	PARTITION;W/AK BOX,PALLET,8355	
412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/	
316675400005	PCB;PWA-8355/BATT ,PROTECTION BD	
316675400002	PCB;PWA-8355/LED TRANS BD	R00
316678300002	PCB;PWA-8555/CHARGER BD	R01
316678300001	PCB;PWA-8555/MOTHER BD	R02
316600000041	PCB;PWA-INVERTER BD (DA1-05A01-A	R0A

Part Number	Description	Location(S)
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222670820003	PE BAG;L560*W345,7521N	
222668820003	PE BUBBLE BAG;160X270MM,ANTI-STA	
222678500002	PE BUBBLE BAG;BATTERY,280*170,MS	
411675400004	PWA;PWA-8355,LED BD	
411678300005	PWA;PWA-8555,CHARGER BD	
411678300009	PWA;PWA-8555H,MOTHER BD	
411678300011	PWA;PWA-8555H,MOTHER BD,SMT	
411678300010	PWA;PWA-8555H,MOTHER BD,T/U	
411676230002	PWA;PWA-BATT,GAUGET BD,SMT,BL436	
411676230001	PWA;PWA-BATT,PROTECT BD,LI,6.6Ah	
411672900001	PWA;PWA-INVERTER BD DA1-05A01	
332810000197	PWR CORD;125V/7A,3P,BLACK,AMERIC	
297212000003	RELAY;REED,200V,.5A,NORMAL OPEN,	SW1
271045037101	RES;.003 ,1W ,1% ,2512,SMT	PR58
271045057101	RES;.005 ,1W,1% ,2512,SMT	PR59
271044060301	RES;.006 ,1.5W,5% ,2512,SMT	RM1
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR561
271045157101	RES;.015 ,1W ,1% ,2512,SMT	PR558
271586026101	RES;.02 ,2W,1%,2512,SMT	PR544,PR554
271045357101	RES;.035,1W,1%,2512,SMT	PR3
271046069101	RES;.06,2W,1%,2512,SMT	PR503,PR504,PR572
271044061101	RES;.06,2W,1%,2512,SMT,乾坤	
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L44,L546,L549,R366,R367,R521,
271061000002	RES;0 ,1/16W,0402,SMT	PR13,PR14,PR16,PR23,PR27,PR3

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Part Number	Description	Location(S)
271071000002	RES;0 ,1/16W,5% ,0603,SMT	L29,L49,L552,L571,PR532,R365
271071000002	RES;0 ,1/16W,5% ,0603,SMT	PR509,PR511,PR7
271071000002	RES;0 ,1/16W,5% ,0603,SMT	R2
271071010301	RES;1 ,1/16W,5% ,0603,SMT	PR1,PR2
271071108101	RES;1.05K,1/16W,1%,0603,SMT	PR512,PR514,PR516
271071124111	RES;1.24K,1/16W,1% ,0603,SMT	PR507
271071122102	RES;1.2K ,1/16W,1% ,0603,SMT	PR502
271071125301	RES;1.2M ,1/16W,5% ,0603,SMT	PR537
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	R25,R26
271061152501	RES;1.5K ,1/16W,5% ,0402,SMT	R357,R648
271071182101	RES;1.8K ,1/16W,1% ,0603,SMT	PR501
271071191101	RES;1.91K, 1/16W,1%,0603,SMT	PR70,PR84
271071100101	RES;10 ,1/16W,1% ,0603,SMT	PR541,PR542
271071100101	RES;10 ,1/16W,1% ,0603,SMT	PR4,PR5
271061100501	RES;10 ,1/16W,5% ,0402,SMT	PR19,PR20,PR21,R157,R163,R167
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R519
271061101103	RES;100 ,1/16W,1% ,0402,SMT	R197,R46,R749
271071101101	RES;100 ,1/16W,1% ,0603,SMT	R128,R142,R617,R72
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R11,R12,R13,R17,R18,R35,R36,R4
271002104301	RES;100K ,1/10W,5% ,0805,SMT	PR569
271061104102	RES;100K ,1/16W,1% ,0402,SMT	PR36,PR57
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR507,PR6,PR9
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R16,R13
271061104501	RES;100K ,1/16W,5% ,0402,SMT	PR22,PR24,PR29,PR3,PR33,PR47
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR514

Part Number	Description	Location(S)
271071107311	RES;107K ,1/16W,1% ,0603,SMT	PR90
271002103301	RES;10K ,1/10W,5% ,0805,SMT	PR10,PR11,PR568,PR570
271061103102	RES;10K ,1/16W,1% ,0402,SMT	PR71,R25,R35,R6,R647,R7
271071103101	RES;10K ,1/16W,1% ,0603,SMT	R8,R18,R19
271061103501	RES;10K ,1/16W,5% ,0402,SMT	PR26,PR46,PR534,PR555,R120,R
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R19,R37,R38
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R297
271061121312	RES;12.1K,1/16W,1% ,0402,SMT	PR52
271071124101	RES;120K ,1/16W,1% ,0603,SMT	R4
271071140101	RES;14 ,1/16W,1% ,0603,SMT	R45
271071150301	RES;15 ,1/16W,5% ,0603,SMT	R9
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R100,R101,R104,R105,R108,R109
271071154101	RES;150K ,1/16W,1% ,0603,SMT	R1
271061152302	RES;15K ,1/16W,5% ,0402,SMT	R243,R244,R266,R709,R710
271071162211	RES;16.2K,1/16W,1% ,0603,SMT	PR37
271071169311	RES;169K ,1/16W,1% ,0603,SMT	PR31
271071174211	RES;17.4K,1/16W,1% ,0603,SMT	PR549
271071181101	RES;180 ,1/16W,1% ,0603,SMT	R103
271071196211	RES;19.6K,1/16W,1% ,0603,SMT	PR510
271061102105	RES;1K ,1/16W,1% ,0402,SMT	PC571,PR1,PR540,PR61,PR72,PR
271071102102	RES;1K ,1/16W,1% ,0603,SMT	R162,R165,R175,R176,R177,R184
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR506
271071102102	RES;1K ,1/16W,1% ,0603,SMT	R14
271061102303	RES;1K ,1/16W,5% ,0402,SMT	PR505,R1,R143,R223,R258,R264,
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R2

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Part Number	Description	Location(S)
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR53
271061105501	RES;1M ,1/16W,5% ,0402,SMT	PR28,PR562,PR563,PR66,PR75,P
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R16,R39
271061221212	RES;2.21K,1/16W,1% ,0402,SMT	R587,R588
271061222501	RES;2.2K ,1/16W,5% ,0402,SMT	R501,R502,R503,R767
271034248301	RES;2.4 ,1/2W ,5% ,2010,SMT	R798
271061249211	RES;2.49K,1/16W,1% ,0402,SMT	R333
271061272102	RES;2.7K ,1/16W,1% ,0402,SMT	R769
271071272101	RES;2.7K ,1/16W,1% ,0603,SMT	PR526
271071201101	RES;200 ,1/16W,1% ,0603,SMT	PR68
271061203102	RES;20K ,1/16W,1% ,0402,SMT	PR41,PR54,PR65,PR78,PR79,PR8
271071203101	RES;20K ,1/16W,1% ,0603,SMT	R30,R17
271061220501	RES;22 ,1/16W,5% ,0402,SMT	R135,R147,R171,R194,R195,R208
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R327
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R41
271071221311	RES;221K ,1/16W,1% ,0603,SMT	PR10
271071223302	RES;22K ,1/16W,5% ,0603,SMT	PR25
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R137
271071274011	RES;274 ,1/16W,1% ,0603,SMT	PR536
271061273501	RES;27K ,1/16W,5% ,0402,SMT	PR38
271061202102	RES;2K ,1/16W,1% ,0402,SMT	R505,R646
271071205101	RES;2M ,1/16W,1% ,0603,SMT	R11
271071324111	RES;3.24K,1/16W,1% ,0603,SMT	PR545
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR40
271071303101	RES;30K ,1/16W,1% ,0603,SMT	R3

Part Number	Description	Location(S)
271061324211	RES;32.4K,1/16W,1% ,0402,SMT	PR56
271071324011	RES;324 ,1/16W,1% ,0603,SMT	R616,R87
271061330501	RES;33 ,1/16W,5% ,0402,SMT	R204,R205,R206,R207,R217,R218
271071330302	RES;33 ,1/16W,5% ,0603,SMT	PR8
271002331301	RES;330 ,1/10W,5% ,0805,SMT	FR3,FR4
271071334301	RES;330K ,1/16W,5% ,0603,SMT	PR551,R799
271071390302	RES;39 ,1/16W,5% ,0603,SMT	R140
271071391302	RES;390 ,1/16W,5% ,0603,SMT	R328
271071393101	RES;39K ,1/16W,1% ,0603,SMT	PR508
271071422111	RES;4.22K,1/16W,1% ,0603,SMT	PR39
271001435301	RES;4.3M,1/10W,5%,0805,SMT	R10
271061475211	RES;4.75K,1/16W,1% ,0402,SMT	PR76,PR81
271071472101	RES;4.7K ,1/16W,1% ,0603,SMT	PR51
271061472501	RES;4.7K ,1/16W,5% ,0402,SMT	R178,R186,R198,R201,R260,R287
271061499212	RES;4.99K,1/16W,1% ,0402,SMT	PR50,R775
271061402011	RES;40.2 ,1/16W,1% ,0402,SMT	R131,R604
271071402311	RES;402K ,1/16W,1% ,0603,SMT	PR55
271071411102	RES;412,1/16W,1% ,0603,SMT	R704
271071442113	RES;44.2 ,1/16W,1% ,0603,SMT	R554
271071442011	RES;442 ,1/16W,1% ,0603,SMT	PR60
271071453211	RES;45.3K,1/16W,1% ,0603,SMT	PR64
271061470101	RES;47, 1/16W, 1%,0402,SMT	R174,R624
271071470102	RES;47.5 , 1/16W,1%,0603,SMT	PR34
271071471101	RES;470 ,1/16W,1% ,0603,SMT	R21,R23,R27
271061471501	RES;470 ,1/16W,5% ,0402,SMT	PR45,R216,R350,R351

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Part Number	Description	Location(S)
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R3,R4,R5,R6,R7
271061474501	RES;470K ,1/16W,5% ,0402,SMT	PR12,PR15,PR17,PR18,PR5,PR6,
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR44,PR552
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR512
271061475111	RES;475 ,1/16W,1% ,0402,SMT	R669
271061473501	RES;47K ,1/16W,5% ,0402,SMT	PR2,PR571,R267,R334,R339,R343
271061499012	RES;49.9 ,1/16W,1% ,0402,SMT	R119,R199,R200,R48,R50
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R250,R555,R558,R567,R642,R650
271061499112	RES;499 ,1/16W,1% ,0402,SMT	R118
271061512102	RES;5.1K ,1/16W,1% ,0402,SMT	PR531,PR77
271061562501	RES;5.6K ,1/16W,5% ,0402,SMT	R254,R692
271002510301	RES;51 ,1/10W,5% ,0805,SMT	R14,R15
271071511812	RES;51.1,1/16W,1% 0603,SMT	R111,R139,R141,R47,R51,R52,R5
271061513302	RES;51K,1/16W,5%,0402,SMT	R259
271071536211	RES;53.6K,1/16W,1% ,0603,SMT	R5
271071560101	RES;56 ,1/16W,1% ,0603,SMT	R102,R565,R574,R93
271061560501	RES;56 ,1/16W,5% ,0402,SMT	R127,R138,R150,R152,R158,R164
271071561101	RES;560 ,1/16W,1% ,0603,SMT	PR506
271071561101	RES;560 ,1/16W,1% ,0603,SMT	R22,R24,R28
271061564101	RES;560K ,1/16W,1% ,0402,SMT	R30,R39,R5,R8
271071563302	RES;56K ,1/16W,5% ,0603,SMT	PR8
271071619811	RES;61.9 ,1/16W,1% ,0603,SMT	R640,R645
271071620102	RES;62,1/16W,1% 0603,SMT	R151,R615,R619
271071622303	RES;620,1/16W,5% ,0603,SMT	R113
271071634211	RES;63.4K,1/16W,1% ,0603,SMT	PR86

Part Number	Description	Location(S)
271061681501	RES;680 ,1/16W,5% ,0402,SMT	R160
271071752101	RES;7.5K ,1/16W,1% ,0603,SMT	PR556
271071713102	RES;715 ,1/16W,1% ,0603,SMT	R112
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R508,R65
271061750501	RES;75 ,1/16W,5% ,0402,SMT	R110,R85,R91,R98
271061753101	RES;75,1/16W,1%,0402,SMT	R159
271071751101	RES;750 ,1/16W,1% ,0603,SMT	R15
271071750311	RES;750K,1/16W,1% ,0603,SMT	PR49
271071806111	RES;8.06K,1/16W,1% ,0603,SMT	PR559,PR73
271061822501	RES;8.2K ,1/16W,5% ,0402,SMT	R146,R148,R149,R154,R155,R156
271071806211	RES;80.6K,1/16W,1% ,0603,SMT	PR550
271071825211	RES;82.5K,1/16W,1% ,0603,SMT	R12,R6,R7
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP561,RP562,RP563,RP564,RP56
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP10,RP48,RP505,RP58,RP597,R
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP4,RP7
271621102302	RP;1K*8 ,10P,1/32W,5% ,1206,SMT	RP6
271561222302	RP;2.2K*8,10P,1/32W,5% ,1608,SMT	RP1,RP2
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP12,RP14,RP16,RP18,RP20,RP2
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP605
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SM	RP584,RP585,RP586,RP587,RP58
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT	RP603
271611473301	RP;47K*4 ,8P ,1/16W,5% ,0612,SMT	RP54,RP55,RP56,RP57,RP608
271621473301	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	RP47,RP606,RP607
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP8,RP9
271611822301	RP;8.2K*4,8P ,1/16W,5% ,0612,SMT	RP53

9. 8555 Spare Part List-12

Part Number	Description	Location(S)
271621822302	RP;8.2K*8,10P,1/32W,5% ,1206,SMT	RP50,RP52
345675400023	RUBBER;DOWN LCD,8355	
345675400044	RUBBER;KB,8355	
345675930001	RUBBER;LCD,UPPER,8677T	
565167830001	S/W;CD ROM,SYSTEM DRIVER,8555	
340675400038	SCREW ASSY;CPU,8355	
371101630301	SCREW;M1.6L3,K-HEAD(+),NIB/NLK	
371101630301	SCREW;M1.6L3,K-HEAD(+),NIB/NLK	
371102011502	SCREW;M2L15,FLT(+),NIW/NLK	
340675400030	SHIELDING ASSY;HDD UP,8355	
342675400017	SHIELDING;HDD TOP,8355	
333020000002	SHRINK TUBE;600V,105'C,D0.8*11.5	
333050000016	SHRINK TUBE;600V,125',D5*15MM,BL	
333025000001	SHRINK TUBE;600V,125℃,Φ2.5mm,L	
333025000001	SHRINK TUBE;600V,125℃,Φ2.5mm,L	
333050000117	SHRINK TUBE;UL,600V,105'C,ID2.5*	
333050000117	SHRINK TUBE;UL,600V,105'C,ID2.5*	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361200003047	SOLDER PASTE;NO CLEAN,RMA,CK3000	
361200003047	SOLDER PASTE;NO CLEAN,RMA,CK3000	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010005	SOLDER WIRE;63/37,0.8,NA,N/C,PRC	
370102611902	SPC-SCREW;M2.6L19,K-HEAD,NIW	

Part Number	Description	Location(S)
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	
370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	
370102010205	SPC-SCREW;M2L2(t0.3),N/W/WLK	
370102010205	SPC-SCREW;M2L2(t0.3),N/W/WLK	
370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,	
370102010303	SPC-SCREW;M2L3,NIW,K-HD(+),NYLOK	
370102010405	SPC-SCREW;M2L4,NIW,K-HD(+),NYLOK	
370102010405	SPC-SCREW;M2L4,NIW,K-HD(+),NYLOK	
370102010606	SPC-SCREW;M2L6,K-HD(t0.2),NIB/NL	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYL	
340678300005	SPEAKER ASSY; L,20*16,2W,MEI-SHA	
340678300006	SPEAKER ASSY; R,20*16,2W,MEI-SHA	
340678300017	SPEAKER ASSY;L,20*16,2W,FENG-CHI	
340678300016	SPEAKER ASSY;R,20*16,2W,FENG-CHI	
226600030332	SPONGE;320*290*10,CAIMAN,PWR	
345668900016	SPONGE;BIOS BATT,M722	
377102610047	S-STANDOFF;M2.6DP3.5H5L1.1,NW	MTG4,MTG5
377102051001	S-STANDOFF;M2DP5H10L1.1,Cu	MTG501
377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	
297040105010	SW;PUSH BUTTOM,5P,SPST,12V/50MA,	SW1
297040200001	SW;PUSH BUTTON,DPDT,4P,12V/50MA	SW8
297040100015	SW;PUSH BUTTON,STS-031,5P,15V/20	SW2,SW3,SW4,SW5,SW6,SW7
225600000419	TAPE; TESA4972, ADHENSIVE, DOUBL	

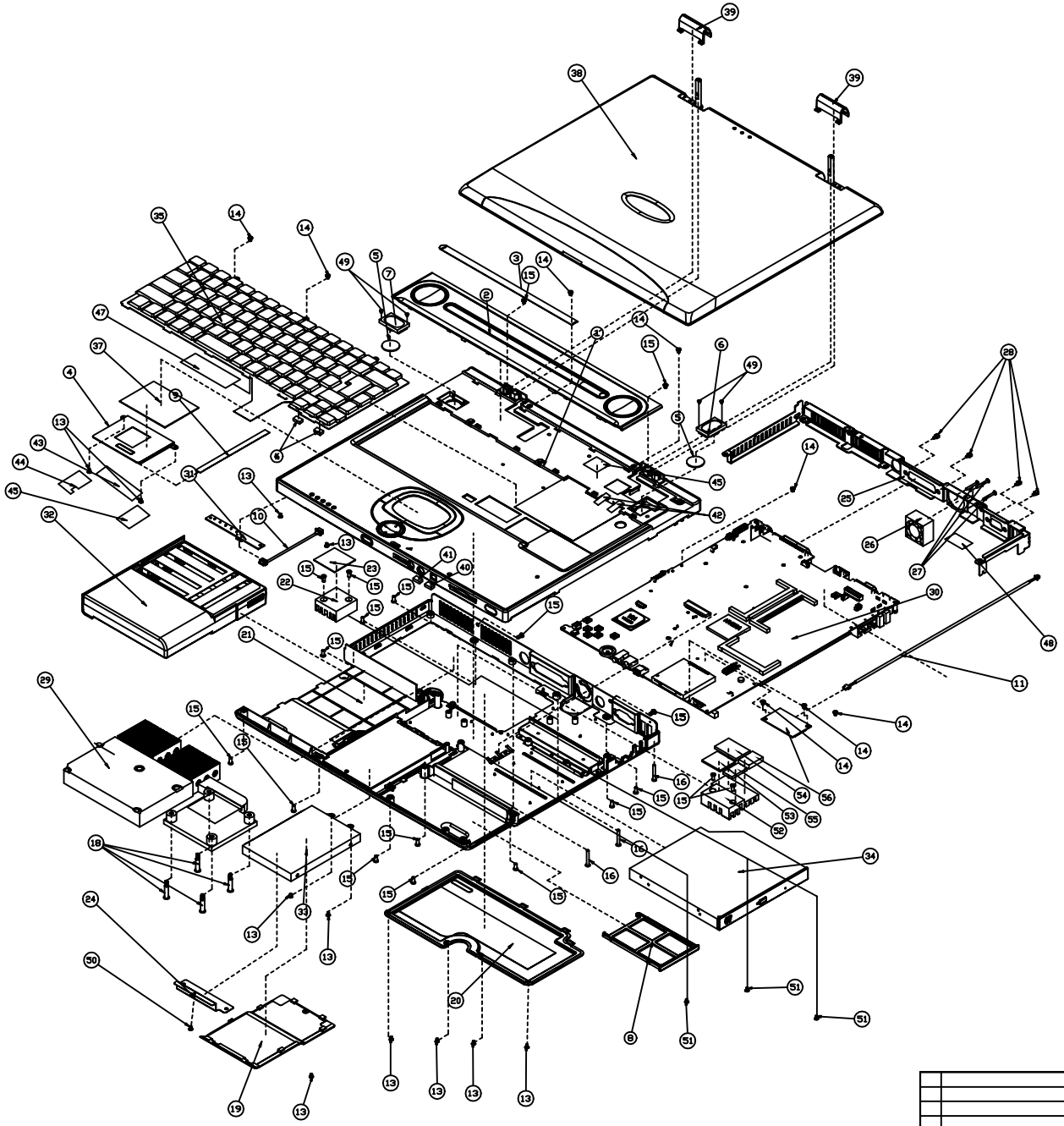
9. 8555 Spare Part List-13

Part Number	Description	Location(S)
225600000403	TAPE;3M,1350F,W=10mm,YELLOW	FOR PCB AND CELL
225600000310	TAPE;ADHENSIVE,DOUBLE-FACE,W8,UL	
225600000054	TAPE;INSULATING,POLYESTER FILM,1	
345675400007	THERMAL PAD;NORTH BRIDGE,MPT,835	
346678300010	THERMAL PAD1;HEATSINK,CHOCK,M/B,	
346678300011	THERMAL PAD2;HEATSINK,CHOCK,M/B,	
346678300016	THERMAL PAD3;HEATSINK,CHOCK,M/B,	
346678300017	THERMAL PAD4;HEATSINK,CHOCK,M/B,	
310111103018	Thermistor;10K,1%,AT-4,80MM	RT2
441675400051	TOUCH PAD MODULE;Synaptics,TM41P	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	PQ1,PQ12,PQ13,PQ15,PQ22,PQ2
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	PQ503
288200301004	TRANS;3LN01S,N-MOSFET,SMCP	Q2
288204532002	TRANS;AP4532M,P&N-MOSFET,SO8	
288200144008	TRANS;DTA144EKA,PNP,SMT	Q8
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	PQ18,Q1,Q10,Q11,Q14,Q4,Q5,Q5
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ14,PQ21
288206035005	TRANS;FDD6035AL,46A,30V,16mOHM,T	PQ503,PQ504,PQ505
288204410004	TRANS;FDS4410,N-MOSFET,SO,8P	PU21,PU3,PU509
288206679003	TRANS;FDS6679,P-MOSFET,.013OHM,S	PQ2,PQ501,PU504,PU505
288207764001	TRANS;FDS7764A,N-MOS,.0075OHM,SO	PU11,PU14
288207764001	TRANS;FDS7764A,N-MOS,.0075OHM,SO	PU501
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	PQ16,Q513,Q514,Q6
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q7
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q1

Part Number	Description	Location(S)
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	PQ19,PQ20,Q503,Q510,Q520,Q52
288202302001	TRANS;SI2302DS,N-MOSFET,SOT-23	Q2
288202303001	TRANS;SI2303DS,P-MOSFET,SOT-23	PQ26
288104362001	TRANS;SI4362DY,N-HOSFET,S08	PQ10,PQ11,PQ3,PQ4,PQ5,PQ6,P
288204410001	TRANS;SI4410DY,N-MOSFET,.02OHM,S	
288204410001	TRANS;SI4410DY,N-MOSFET,.02OHM,S	PU503
288204532001	TRANS;SI4532DY,N&P-MOSFET,SO8,PR	U2
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU1,PU18,PU20,PU502
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PU19,PU22,PU501
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	PU2,PU3
288204892001	TRANS;SI4892DY,N-MOSFET,SO8	PU12,PU13
288200610001	TRANS;TP0610T,P-MOSFET,SOT-23	PQ17
288208107001	TRANS;TPC8107,13A/30V,P-MOSFET,S	Q10,Q11,Q12,Q13,Q14,Q9
373101713001	T-SCREW;B,M1.7L3,K-HD,T=0.5,0,NI	
270140000003	VARISTOR;280V,5.6X3.8MM,TVB280-0	S1
271911103906	VR;10K,20%,0.05W,RN101GAC10KPHJ-	VR1
421675400011	WIRE ASSY;ANTENNA,HSD,LCD,8355	
421675400008	WIRE ASSY;ANTENNA,H-T,LCD,8355	
421675400012	WIRE ASSY;BIOS,BATTERY,8355	
421675400001	WIRE ASSY;INVERTER,8355	
421678300007	WIRE ASSY;INVERTER,8555	
421678300001	WIRE ASSY;LCD,QD141X1LH12,8555	
421678300008	WIRE ASSY;LCD,QD141X1LH12,8555	
421675400009	WIRE ASSY;LED BD,TOP,8355	
421675400010	WIRE ASSY;MDC,8355	

9. 8555 Spare Part List-14

Part Number	Description	Location(S)
421678300013	WIRE ASSY;MDC,H-T,8555	
422676200004	WIRE; UL1007 #20 AWG, 41mm, RED;	CN10
422676200002	WIRE; UL1007 #20 AWG, 45mm, BLUE	
422676200006	WIRE; UL1007 #20 AWG, 84mm, BLAC	CN6
422676200001	WIRE; UL1007 #20 AWG, 90mm, BLUE	
422676200008	WIRE; UL1007 #26 AWG, 122mm, BLU	CN8
422676200007	WIRE; UL1007 #26 AWG, 51mm, YELL	CN9
422676200005	WIRE; UL1007 #26 AWG, 62mm, BROW	CN7
273001050080	XFMR;CI8.5,16T/2600T,220mH,SMT,o	T1
273001050081	XFMR;CI8.5,16T/2600T,220mH,SMT,o	
273001050028	XSFORMER;10/100 BASE,LF-H41S,SMT	U509
274011200411	XTAL;12MHz,30PPM,16PF,8*4.5,2P,S	X3
274011431422	XTAL;14.318MHZ,16PF,20PPM,8*4.25	X2
274011431443	XTAL;14.318MHz,20PPM,16PF,8*4.5,	
274011600418	XTAL;16MHZ,16PF,30PPM,8*4.5,2P,E	
274011600408	XTAL;16MHZ,16PF,50PPM,8*4.5,2P	X5
274012457426	X'TAL;24.576MHZ,16PF,30ppm,8*4.5	
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	X7,X8
274012500420	XTAL;25MHz,30PPM,16PF,8*4.5,2P,S	X4,X9
274012700407	X'TAL;27.00MHZ,20PF,20ppm,8*4.5,	
274012700406	XTAL;27MHZ,20PF,20PPM,8.0*4.5,SM	X1
274013276114	XTAL;32.768KHZ,10PPM,12.5PF	X6
		P/N:526267833001



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
56	370102010405	THERMAL PAD4;HEATSINK,CHOCK,M/B,8555	1	PART	
55	370102010205	THERMAL PAD3;HEATSINK,CHOCK,M/B,8555	1	PART	
54	371101630301	THERMAL PAD2;HEATSINK,CHOCK,M/B,8555	1	PART	
53	346675400029	THERMAL PAD1;HEATSINK,CHOCK,M/B,8555	1	PART	
52	343678300001	HEATSINK;MOS,8555,MPT	1	PART	
51	370102010405	SPC-SCREW;M2L4,NIW,K-HD(+),NYLOK	3	PART	
50	370102010205	SPC-SCREW;M2L2<t0.3),NIW/WLK	1	PART	
49	371101630301	SCREW;M1.6L3,K-HD(+),NIB/NLK	4	PART	
48	346675400029	CONDUCTIVE TAPE;DC-IN,MB,8355	1	PART	
47	346675400028	CONDUCTIVE TAPE;KB,8355	1	PART	
46	345675400030	GASKET;KB,8355	2	PART	
45	345678300013	CONDUCTIVE TAPE;TP BRACKET,RIGHT,8555,ID1	2	PART	
44	345678300012	CONDUCTIVE TAPE;TP BRACKET,LEFT,8555,ID1	1	PART	
43	345678300011	CONDUCTIVE TAPE;TP BRACKET,UP,8555,ID1	1	PART	
~~42~~	~~225675400001~~	~~CONDUCTIVE TAPE;TOP ASSY,DDR,RIGHT,8355~~	~~2~~	~~PART~~	
41	345675400012	GASKET;M/B ASSY,MIC-IN,8355	1	PART	
40	345675400011	GASKET;M/B ASSY,1394,8355	1	PART	
39	344675400016	COVER;HINGE,8355	2	PART	
38	441675400031	LCD ASSY;14"XGA,QDI,8355	1	ASSY	
37	441675400051	TOUCH PAD MODULE;Synaptics,TM41P	1	PART	
36	412672300001	PCB ASSY;FAX MODEM 56K,MDC56S-I	1	ASSY	
35	531017240112	KBD;88,US,3000170042,ZIPPY,8355	1	ASSY	
34	451675400071	CD-ROM TEAC ME KIT;8355	1	ASSY	
33	451675400111	HDD ME KIT;8355	1	ASSY	
32	441676200001	BATT ASS'Y;14.8V,6.6AH,LI,BL4366G03	1	ASSY	MSL
31	411675400004	PWA;PWA-8355,LED BD	1	ASSY	MSL
30	411675400001	PWA;PWA-8355,MOTHER BD,T/U	1	ASSY	MSL
29	340675400024	HEATSINK ASSY;CPU,AMD KB DTM,8355	1	ASSY	MPT
28	377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	4	PART	
27	371102011502	SCREW;M2L15 FLT(+) NIW/NLK	3	PART	
26	340675400029	FAN ASSY;ID,8355	1	ASSY	SUNON
25	342675400013	BRACKET;ID,8355	1	PART	MPT
24	342675400017	SHIELDING;HDD TOP,8355	1	PART	MPT
23	345675400007	THERMAL PAD;NB,DV,8355,MPT	1	PART	MPT
22	343675400003	HEATSINK;NB,8355,MPT	1	PART	MPT
21	340678300013	HOUSING ASSY;HOUSING,8555	1	ASSY	ShenJI
20	340675400014	COVER ASSY;CPU,8355	1	ASSY	ShenJI
19	344675400024	COVER;HDD,8355	1	PART	ShenJI
18	340672400009	SCREW ASSY;CPU,8640S	4	ASSY	
17	370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYLOK	2	PART	
16	370102611902	SPC-SCREW;M2.6L19,K-HEAD,NIW	3	PART	
15	370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	17	PART	
14	370102610302	SPC-SCREW;M2.6L3 NIB,K-HD,NYLOK	8	PART	
13	370102010303	SPC-SCREW;M2L3,NIW,K-HD(+),NYLOK	11	PART	
~~12~~	~~346675400025~~	~~PAD;CHOCK,M/B,8355~~	~~1~~	~~PART~~	~~MPT~~
11	421675400010	WIRE ASSY;MDC,8355	1	ASSY	MPT
10	421675400009	WIRE ASY;LED BD,TOP,8355	1	ASSY	MPT
9	422675400001	FFC ASSY;TOUCH-PAD,8355	1	PART	??
8	344672300025	DUMMY CARD;PCMCIA,MANGUSTA	1	PART	MPT
7	340678300005	SPEAKER ASSY;L,20*16*2W,MEI-SHAN,8555	1	ASSY	??
6	340678300006	SPEAKER ASSY;R,20*16,,2W,MEI-SHAN,8555	1	ASSY	??
~~5~~	~~345675400004~~	~~SPONGE,SPEAKER,8355~~	~~2~~	~~PART~~	~~MPT~~
4	340675400011	BRACKET ASSY;TOUCH-PAD,8355	1	ASSY	MPT
3	344675400015	NAME-PLATE,SPEAKER COVER,8355	1	PART	ShenJI
2	340675400010	COVER ASSY;SPEAKER,K/B,8355	1	ASSY	ShenJI
1	340678300002	COVER ASSY;TOP,8555	1	ASSY	ShenJI

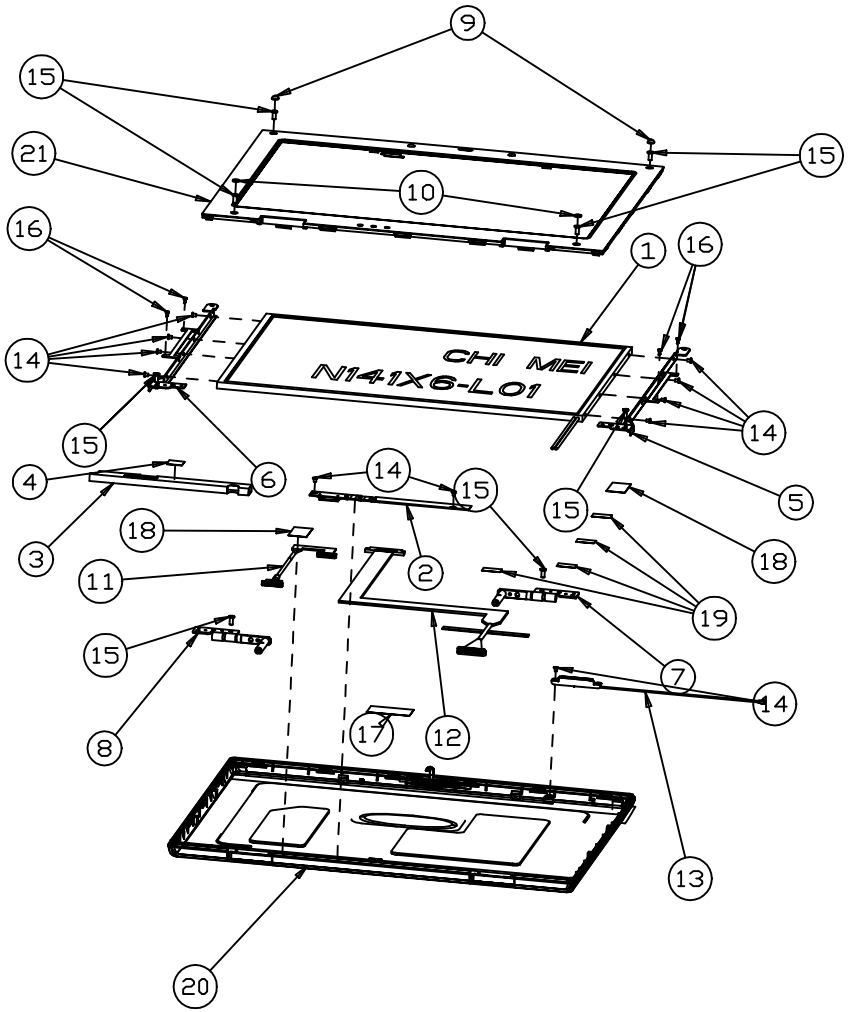
ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

TOL.± RANGE	M1	M2	S1	S2	P1	P2	C	B
0~6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6~30	0.1	0.2	.15	.25	0.1	.15	1	.15
30~80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80~180	.15	0.3	.25	.45	0.4	0.8	3	.25
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315~800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

DATE	20-Feb-03	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.500	DRAWING NAME	8555 CASE KIT		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	526267830001	R00A

MiTAC Technology Corp.

SHEET NO. 1 OF 1



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
21	340675400004	COVER ASSY;LCD 14",8355	1	ASSY	
20	340675400003	HOUSING ASSY;LCD 15",8355	1	ASSY	
19	225675400001	CONDUCTIVE TAPE;TOP ASSY,DDR RIGHT,8355	4	PART	
18	345678300013	CONDUCTIVE TAPE;TP BRACKET,RIGHT,8555,ID1	2	PART	
17	345678300022	CONDUCTIVE TAPE;LCD PANEL,8555	1	PART	
16	371101630301	SCREW;M1.6L3,K-HEAD(+),NIB/NLK	4	PART	
15	370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	8	PART	
14	370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,NIW	11	PART	
13	421675400008	WIRE ASSY;ANTENNA,H-T,LCD,8355	1	ASSY	
12	421675400006	WIRE ASSY;LCD,Chi-mei,N141X6-L01,8355	1	ASSY	
11	421675400001	WIRE ASSY;INVERTER,8355	1	ASSY	
10	345675400023	RUBBER;DOWN LCD,8355	2	PART	
9	345675930001	RUBBER;LCD,UPPER,8677T	2	PART	
8	340675400002	HINGE;L,14",8355	1	ASSY	
7	340675400001	HINGE;R,14",8355	1	ASSY	
6	342675400002	BRACKET;LCD 14",L,8355	1	PART	
5	342675400001	BRACKET;LCD 14",R,8355	1	PART	
4	242664800013	LABEL;CAUTION,INVERT BD,PITCHING	1	PART	
3	346669900004	INSULATOR;INVERTER,7170	1	PART	
2	411672900001	PWA;PWA-INVERTER BD DAI-05A01	1	ASSY	
1	413000020321	LCD;N141X6-L01,TFT,14",LVDS,XGA,CHIMEI	1	PART	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

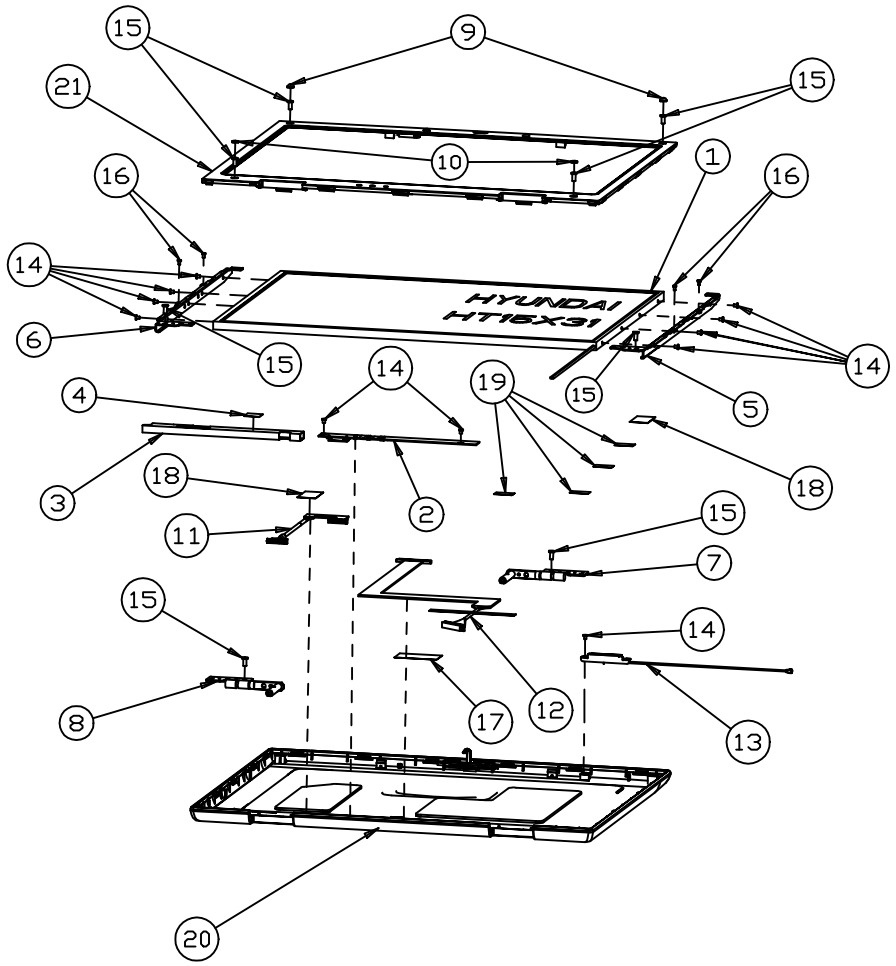
TOL± / RANGE	Pla.	Met.	Ins.	Por.	Cab.	Pac.	Gas.	PCB
0~6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6~30	0.1	0.1	.15	.25	1	1	0.5	0.1
30~80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80~180	.15	.15	.25	0.3	2	2	1	.15
180~315	.15	0.2	0.3	0.4	2.5	2	1	.15
315~800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	19-Sep-03	MATERIAL	SEE NOTES	TREATMENT		REMARK
UNIT	MM	SCALE	0.250	DRAWING NAME	LCD ASSY;14",XGA,Chi-mei,8355 ID1	
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	441675400032 R00

MiTAC Technology Corp.

model nameLCD-ASSY-14-8355

file nameLCD_ASSY_CHIMEI14_ID1_8355



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
21	340675400007	COVER ASSY;LCD 15",8355	1	ASSY	
20	340675400003	HOUSING ASSY;LCD 15",8355	1	ASSY	
19	225675400001	CONDUCTIVE TAPE;TOP ASSY,DDR RIGHT,8355	4	PART	
18	345678300013	CONDUCTIVE TAPE;TP BRACKET,RIGHT,8555,ID1	2	PART	
17	345678300022	CONDUCTIVE TAPE;LCD PANEL,8555	1	PART	
16	371101630301	SCREW;M1.6L3,K-HEAD(+),NIB/NLK	4	PART	
15	370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	8	PART	
14	370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,NIW	11	PART	
13	421675400008	WIRE ASSY;ANTENNA,H-T,LCD,8355	1	ASSY	
12	421675400003	WIRE ASSY;LCD,HYUNDA,HT15X31-100,8355	1	ASSY	
11	421675400001	WIRE ASSY;INVERTER,8355	1	ASSY	
10	345675400023	RUBBER;DOWN LCD,8355	2	PART	
9	345675930001	RUBBER;LCD,UPPER,8677T	2	PART	
8	340675400006	HINGE;L,15",8355	1	ASSY	
7	340675400005	HINGE;R,15",8355	1	ASSY	
6	342675400004	BRACKET;LCD 15",L,8355	1	PART	
5	342675400003	BRACKET;LCD 15",R,8355	1	PART	
4	242664800013	LABEL;CAUTION,INVERT BD,PITCHING	1	PART	
3	346669900004	INSULATOR;INVERTER,7170	1	PART	
2	411672900001	PWA;PWA-INVERTER BD DAI-05A01	1	ASSY	
1	413000020360	LCD; HT15X31-100,TFT,15",LVDS,XGA,HYDIS	1	PART	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

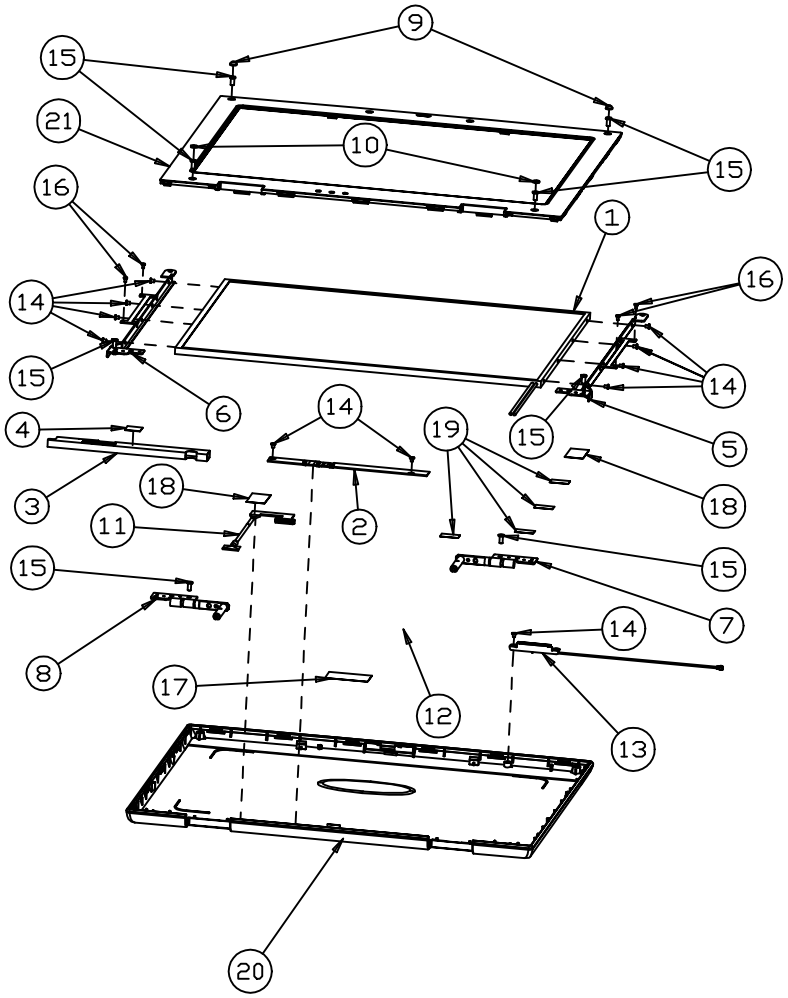
TOL± RANGE	Pla.	Met.	Ins.	Por.	Cab.	Pac.	Gas.	PCB
0~6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6~30	0.1	0.1	.15	.25	1	1	0.5	0.1
30~80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80~180	.15	.15	.25	0.3	2	2	1	.15
180~315	.15	0.2	0.3	0.4	2.5	2	1	.15
315~800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	19-Sep-03	MATERIAL	SEE NOTES	TREATMENT		REMARK
UNIT	MM	SCALE	0.250	DRAWING NAME	LCD ASSY;15",XGA,Hyundai,8355 ID1	
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	441675400034 R00

MiTAC Technology Corp.

model nameLCD-ASSY-15-8355

file nameLCD_ASSY_HYUNDAI15_ID1_8355



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
21	340675400004	COVER ASSY;LCD 14",8355	1	ASSY	
20	340675400003	HOUSING ASSY;LCD 15",8355	1	ASSY	
19	225675400001	CONDUCTIVE TAPE;TOP ASSY,DDR RIGHT,8355	4	PART	
18	345678300013	CONDUCTIVE TAPE;TP BRACKET,RIGHT,8555,ID1	2	PART	
17	345678300022	CONDUCTIVE TAPE;LCD PANEL,8555	1	PART	
16	371101630301	SCREW;M1.6L3,K-HEAD(+),NIB/NLK	4	PART	
15	370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	8	PART	
14	370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,NIW	11	PART	
13	421675400008	WIRE ASSY;ANTENNA,H-T,LCD,8355	1	ASSY	
12	421675400007	WIRE ASSY;LCD,AU-B141XN04-2,8355	1	ASSY	
11	421675400001	WIRE ASSY;INVERTER,8355	1	ASSY	
10	345675400023	RUBBER;DOWN LCD,8355	2	PART	
9	345675930001	RUBBER;LCD,UPPER,8677T	2	PART	
8	340675400002	HINGE;L,14",8355	1	ASSY	
7	340675400001	HINGE;R,14",8355	1	ASSY	
6	342675400002	BRACKET;LCD 14",L,8355	1	PART	
5	342675400001	BRACKET;LCD 14",R,8355	1	PART	
4	242664800013	LABEL;CAUTION,INVERT BD,PITCHING	1	PART	
3	346669900004	INSULATOR;INVERTER,7170	1	PART	
2	411672900001	PWA;PWA-INVERTER BD DAI-05A01	1	ASSY	
1	413000020323	LCD;B141XN04-2,TFT,14",LCDS,XGA,AUO	1	PART	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

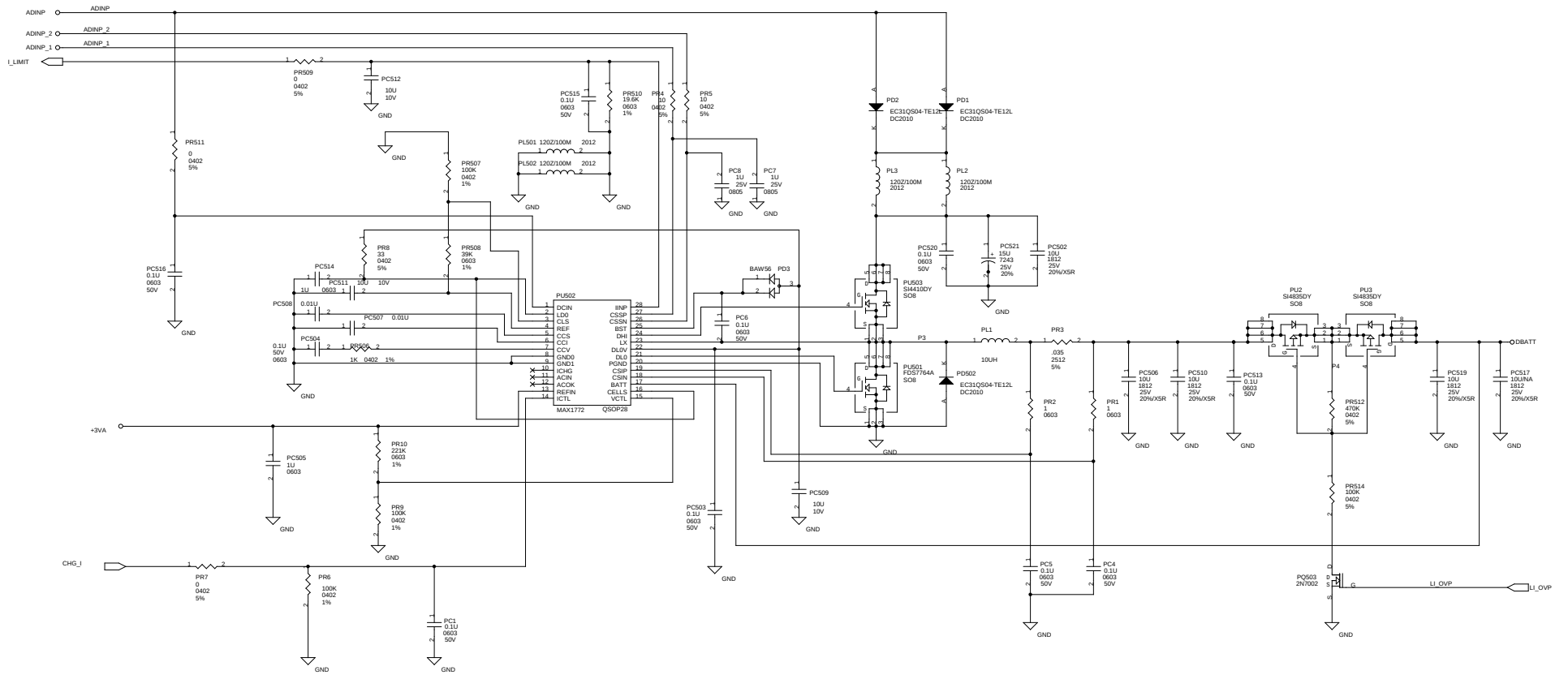
TOL± RANGE	Pla	Met	Ins	Por	Cab	Pac	Gas	PCB
0~6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6~30	0.1	0.1	.15	.25	1	1	0.5	0.1
30~80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80~180	.15	.15	.25	0.3	2	2	1	.15
180~315	.15	0.2	0.3	0.4	2.5	2	1	.15
315~800	0.2	0.3	0.4	0.5	3	3	2	.15

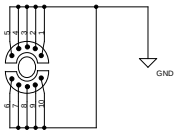
DATE	19-Sep-03	MATERIAL	SEE NOTES	TREATMENT		REMARK
UNIT	MM	SCALE	0.250	DRAWING NAME	LCD ASSY;14",XGA,AU,8355 ID1	
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	441675400033 R00

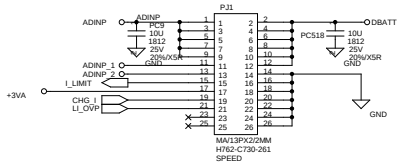
MiTAC Technology Corp.

model nameLCD-ASSY-14-8355

file nameLCD_ASSY_AUO14_ID1_8355







MiTAC		
Title	DC-DC CONNECTOR ,CHARGER	
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Date: 日, 一, 二, 四 29, 2003	Sheet 1 of 1	

MODEL : 8555 Revision 0B

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POWER STATES

STATE / SIGNAL	VOTAGE	POWER ON	STR	STD	MEC-OFF	REMARK
H8_SUSB	-	HIGH	LOW	LOW	LOW	
H8_SUSC	-	HIGH	HIGH	LOW	LOW	
ADP	+19V	O	O	O	O	
BATTERY	+12V	O	O	O	O	
+VCC_CORE	+1.75V	O	X	X	X	
+12V	+12V	O	O	X	X	
+12VS	+12V	O	X	X	X	
+5V	+5V	O	O	X	X	
+5VS	+5V	O	X	X	X	
+3V	+3.3V	O	O	X	X	
+3VS	+3.3V	O	X	X	X	
+2.5V_DDR	+2.5V	O	O	X	X	
VDD_MEM2.5	+2.5V	O	X	X	X	
+1.8V	+1.8V	O	O	X	X	
+1.8VS	+1.8V	O	X	X	X	
+1.5V	+1.5V	O	O	X	X	
+1.5VS	+1.5V	O	X	X	X	
+1.25VS_DDR	+1.25V	O	X	X	X	
+1.2VS	+1.2V	O	X	X	X	
+5VA	+5V	O	O	O	O	
+5VAS	+5V	O	O	O	X	
+3VA	+3.3V	O	O	O	O	

IDSEL

IDSEL	CHIP
AD11	SiS 963
AD12	PCI to PCI Bridge
AD13	IEEE1394
AD13	AC'97 Codec
AD13	Super I/O
AD14	USB
AD15	MII
AD16/17	ATI M10P/ ATI M9+X
AD20	CB710
AD21	MiniPCI

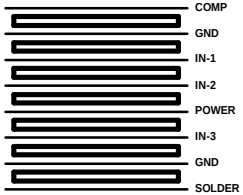
BUS MASTER

REQ/GNT	CHIP
-REQ0/-GNT0	CB710
-REQ2/-GNT2	MINI PCI

PCIINT

PCIINT	CHIP
INTA#	SISM661/ ATIM10P/ ATIM9+X/ SIS302LV
INTB#	PCMCIA (CB710)
INTC#	PCMCIA (CB710)
INTC#	MINI PCI
INTD#	MINI PCI

Board Stackup-up



DRAW	DESIGN	CHECK	ISSUED

MiTAC

Title: COVER SHEET

Size | Document Number: 411678300001 | Rev: R0A

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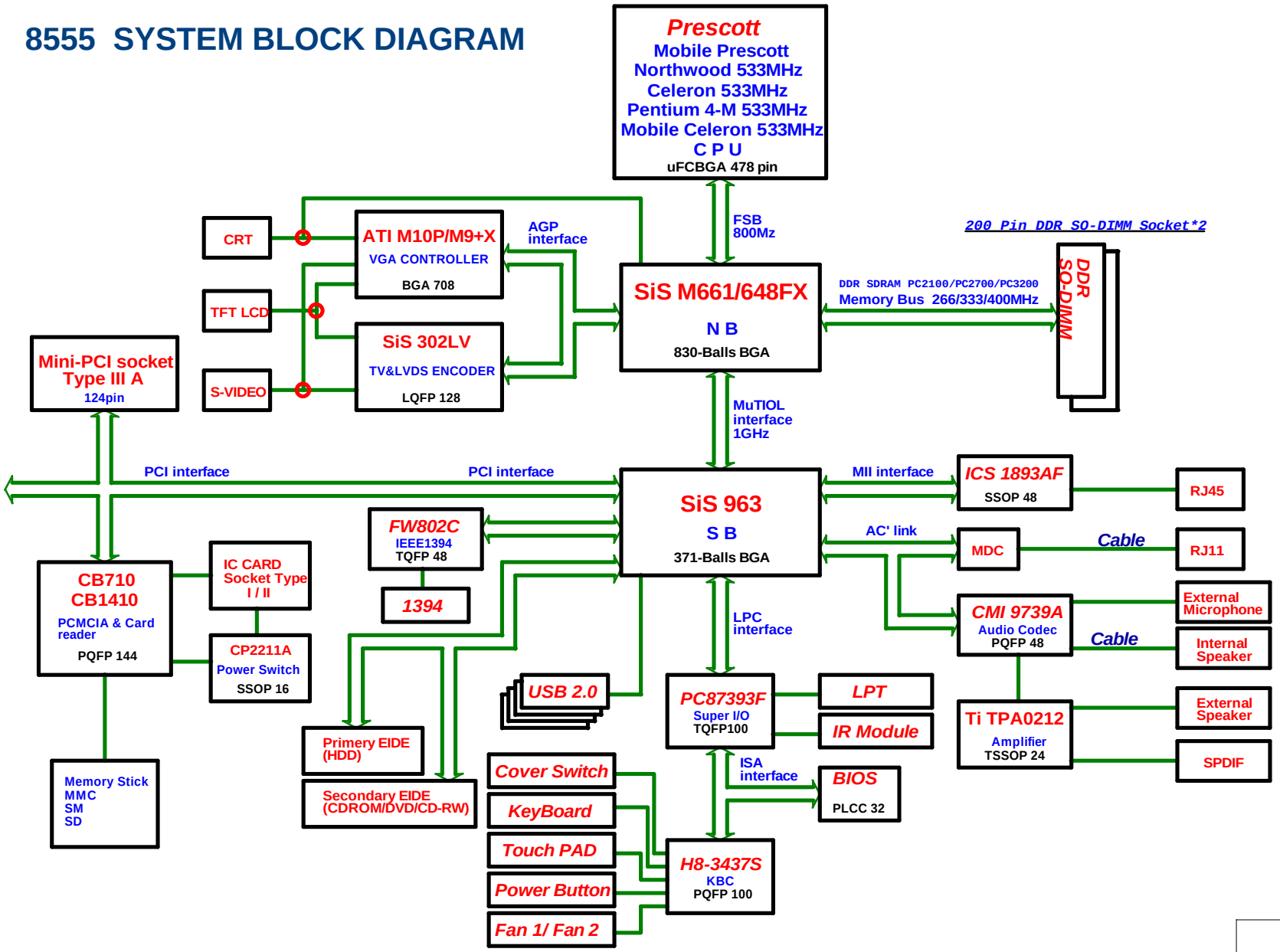
8555 SYSTEM BLOCK DIAGRAM



MiTAC

Title	SystemBlock DIAGRAM	
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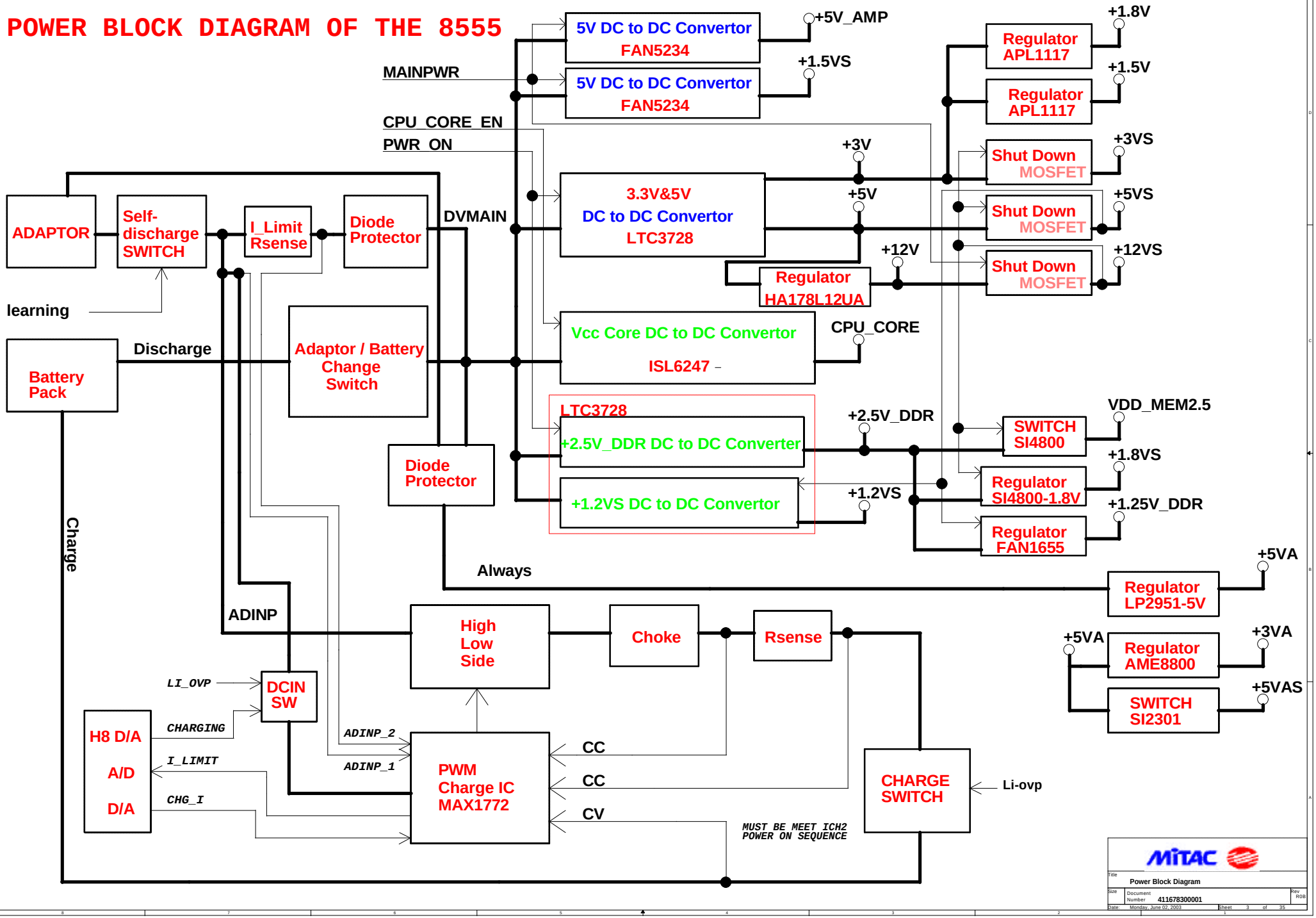
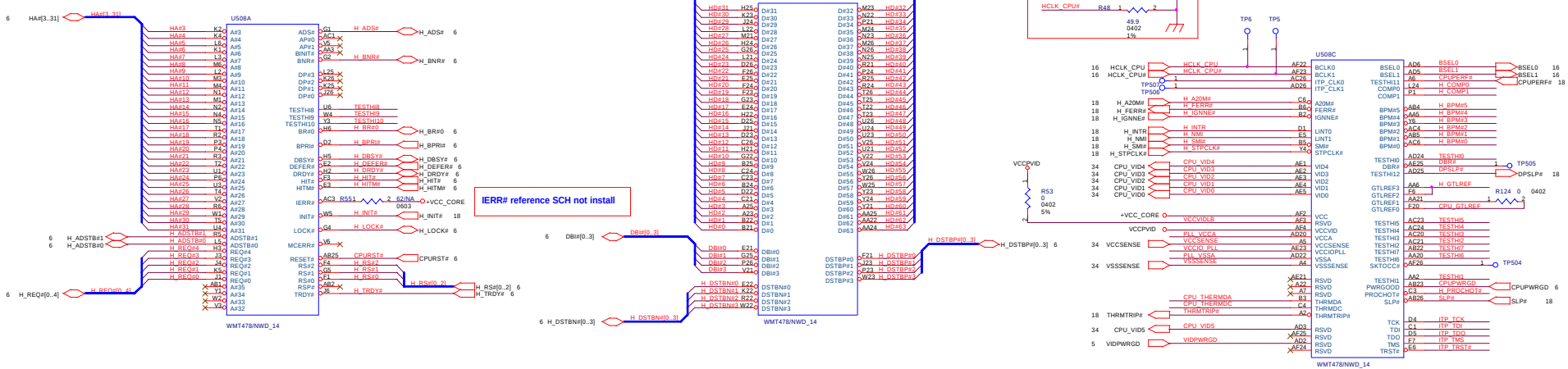
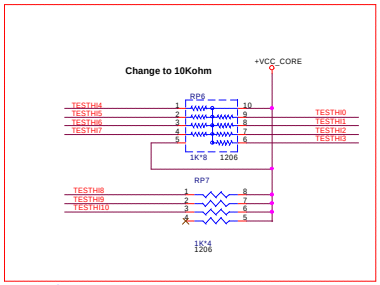
POWER BLOCK DIAGRAM OF THE 8555

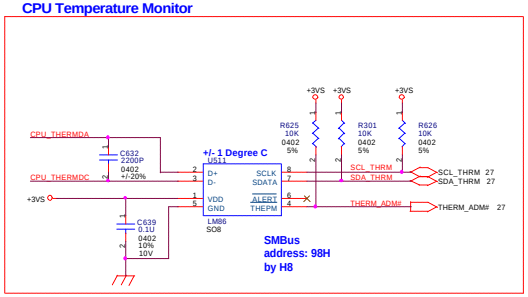


Prescott/Northwood (1/2)

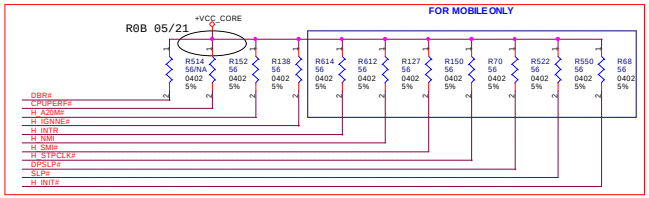




CPU Temperature Monitor

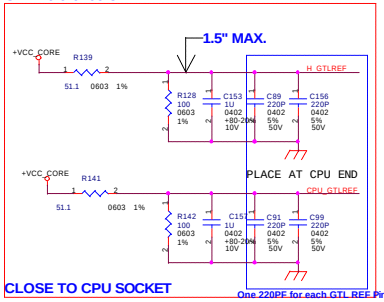


Placement : 3" (Maximum) From CPU

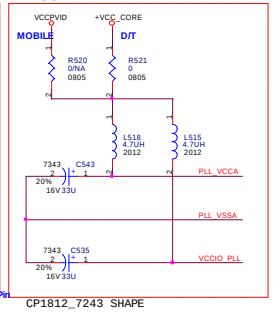


R? must be pull hi at DT.Because the signal was input of TEST_HI12.

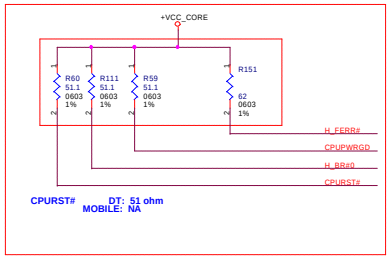
GTL Reference CKT



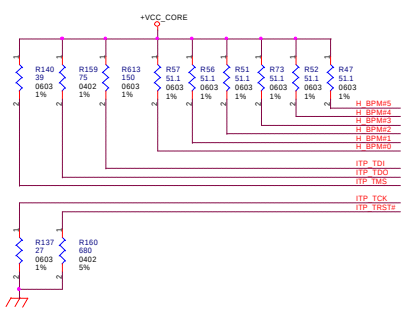
PLL SUPPLY FILTER



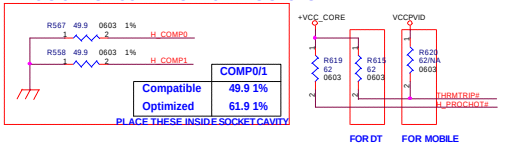
CPU SIGNAL TERMINATION



PLACE CLOSE TO CPU SOCKET



PRECISION FSB COMPENSATION RESISTORS



MiTAC

Title	Prescott/Northwood (1/2)	
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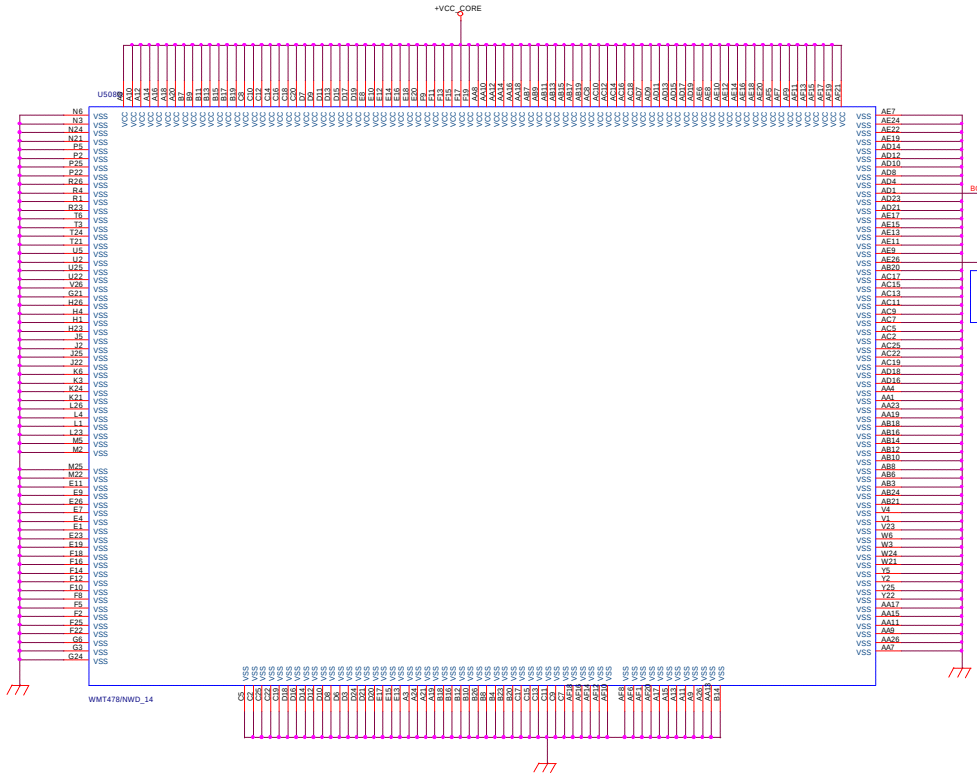
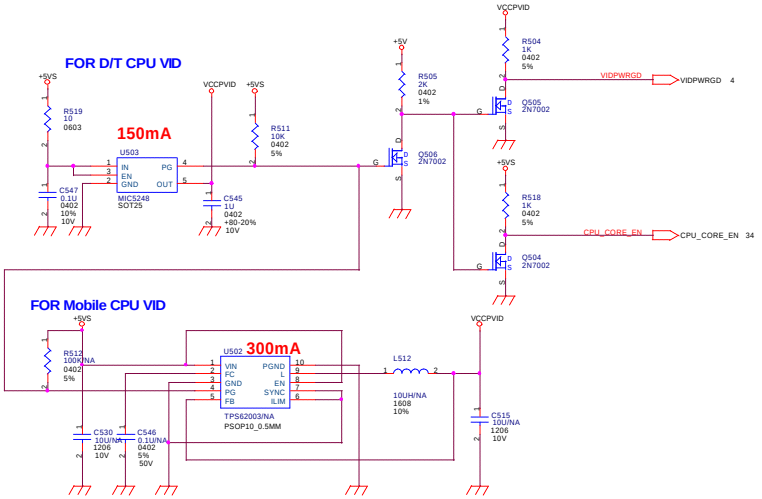
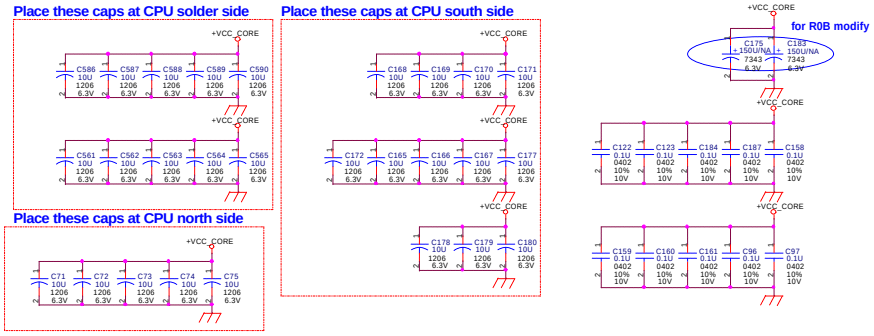
Prescott/Northwood (2/2)






Place these caps at CPU solder side
Place these caps at CPU south side
Place these caps at CPU north side
for R0B modify
+VCC_CORE
C506 C587 C588 C589 C590 C561 C562 C563 C564 C565
C168 C169 C170 C171 C172 C165 C166 C167 C177 C178 C179 C180
C175 150U/NA 7343 6.3V
C183 150U/NA 7343 6.3V
C122 C123 C184 C187 C158 C159 C160 C161 C96 C97
C71 C72 C73 C74 C75
10U 1206 6.3V
0.1U 0402 10% 10V

10U/6.3V change to 22U/6.3V within CPU +VCC_CORE

MiTAC

Title	Prescott/Northwood (2/2)	
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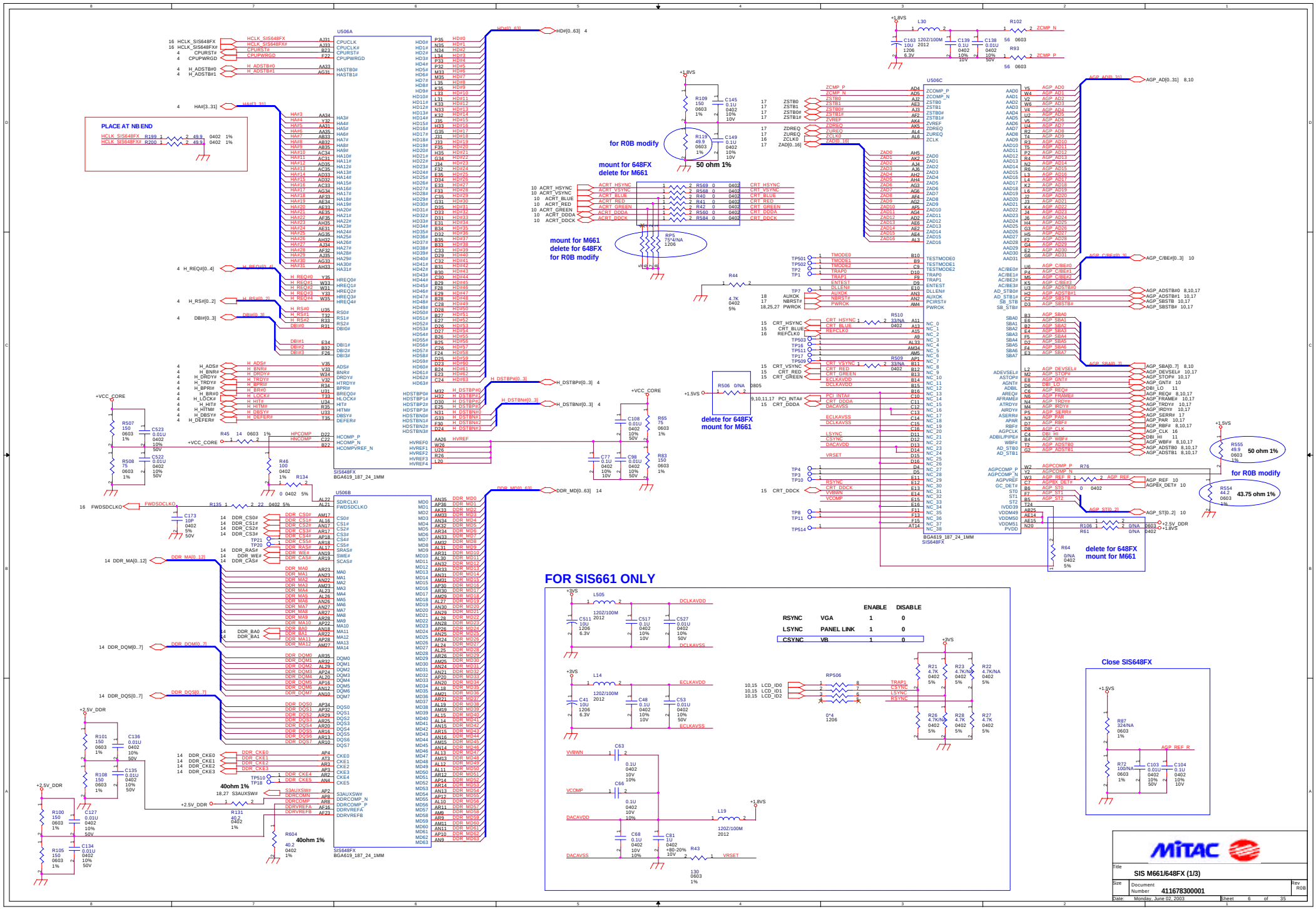
PLACE AT NB END
HCLK_SIS648FX R199 1 2 49.9 0402 1%
HCLK_SIS648FX# R200 1 2 49.9 0402 1%
U506A
SIS648FX
BGA619_187_24_1MM
U506B
SIS648FX
BGA619_187_24_1MM
U506C
SIS648FX
BGA619_187_24_1MM
for R0B modify
50 ohm 1%
mount for 648FX
delete for M661
mount for M661
delete for 648FX
for R0B modify
delete for 648FX
mount for M661
40ohm 1%
40ohm 1%
FOR SIS661 ONLY
ENABLE DISABLE
RSYNC VGA 1 0
LSYNC PANEL LINK 1 0
CSYNC VB 1 0
Close SIS648FX
for R0B modify
43.75 ohm 1%
MiTAC
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SIS M661/648FX (1/3)
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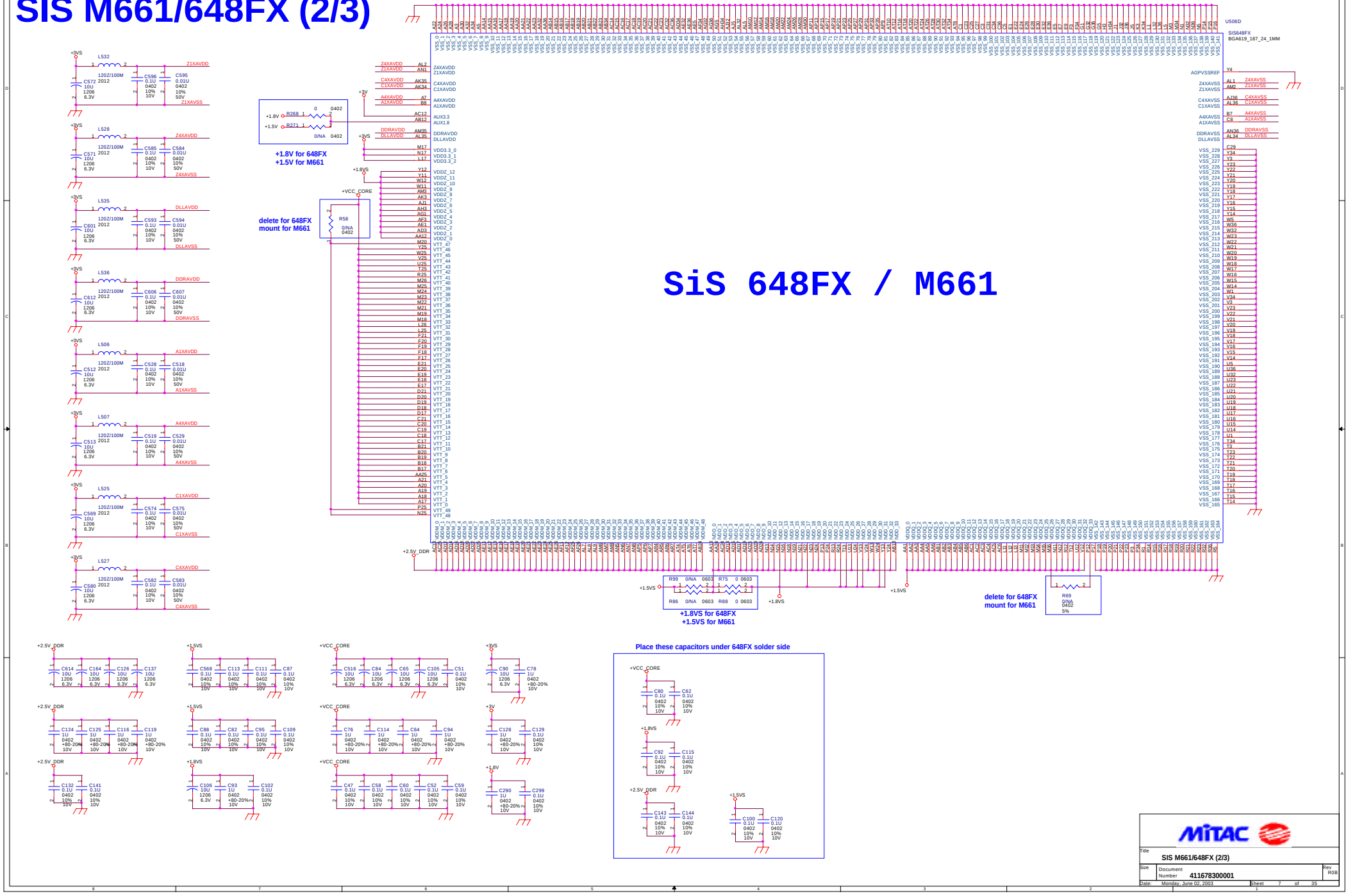
SIS M661/648FX (2/3)



Title	SIS M661/648FX (2/3)
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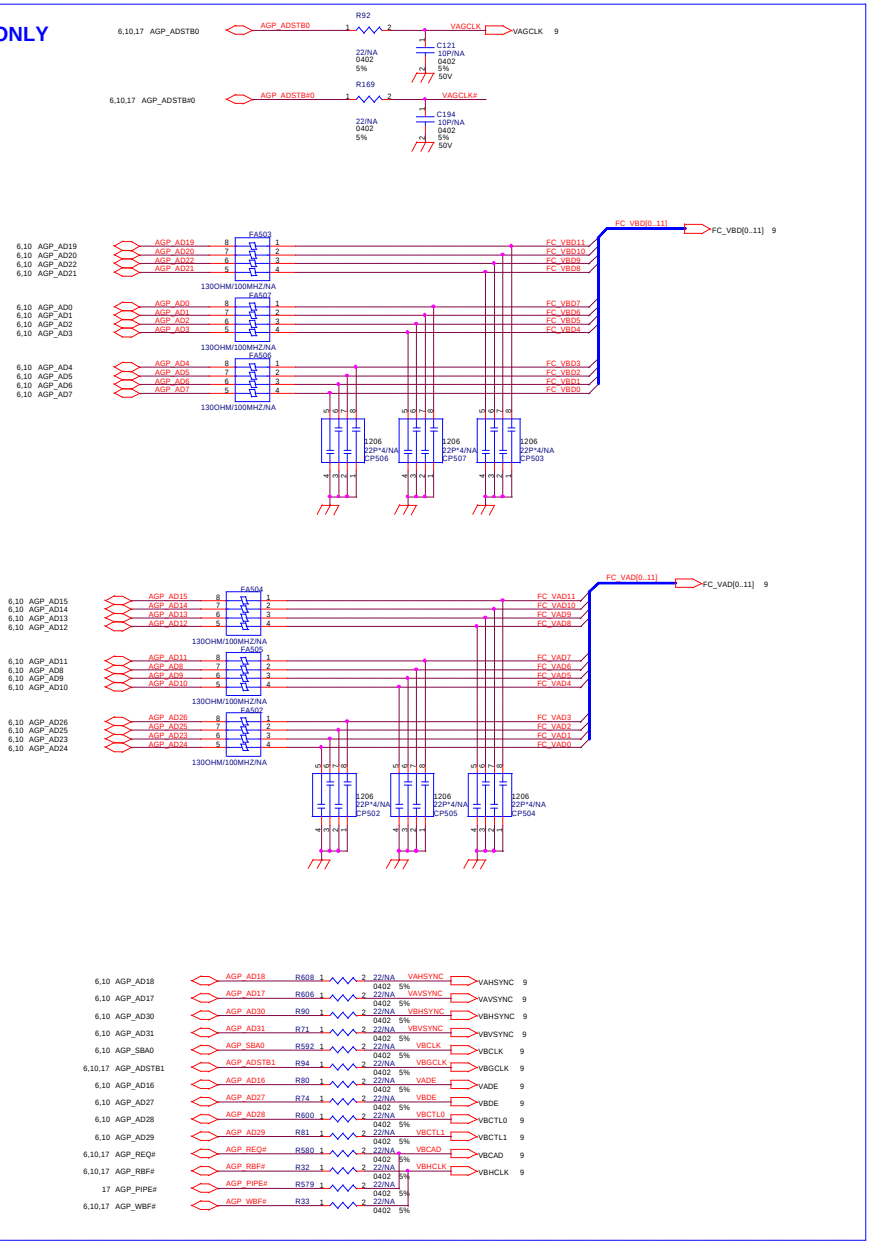
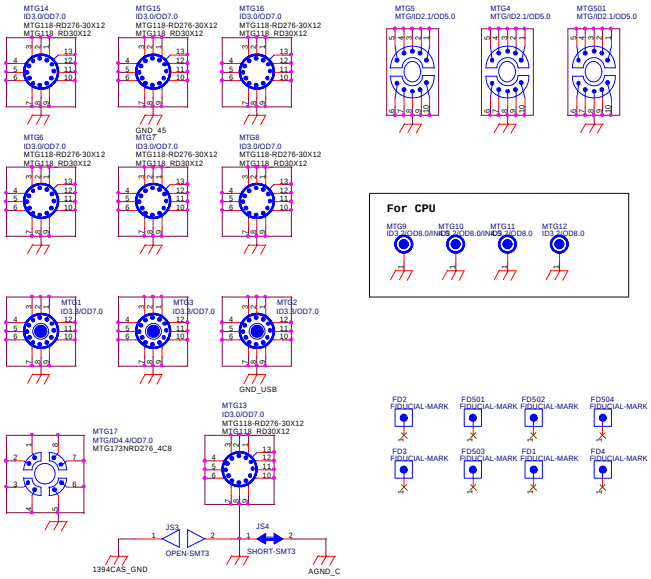
SIS M661/648FX (3/3)

FOR SIS661 ONLY





MiTAC

Title	SIS M661/648FX (3/3)
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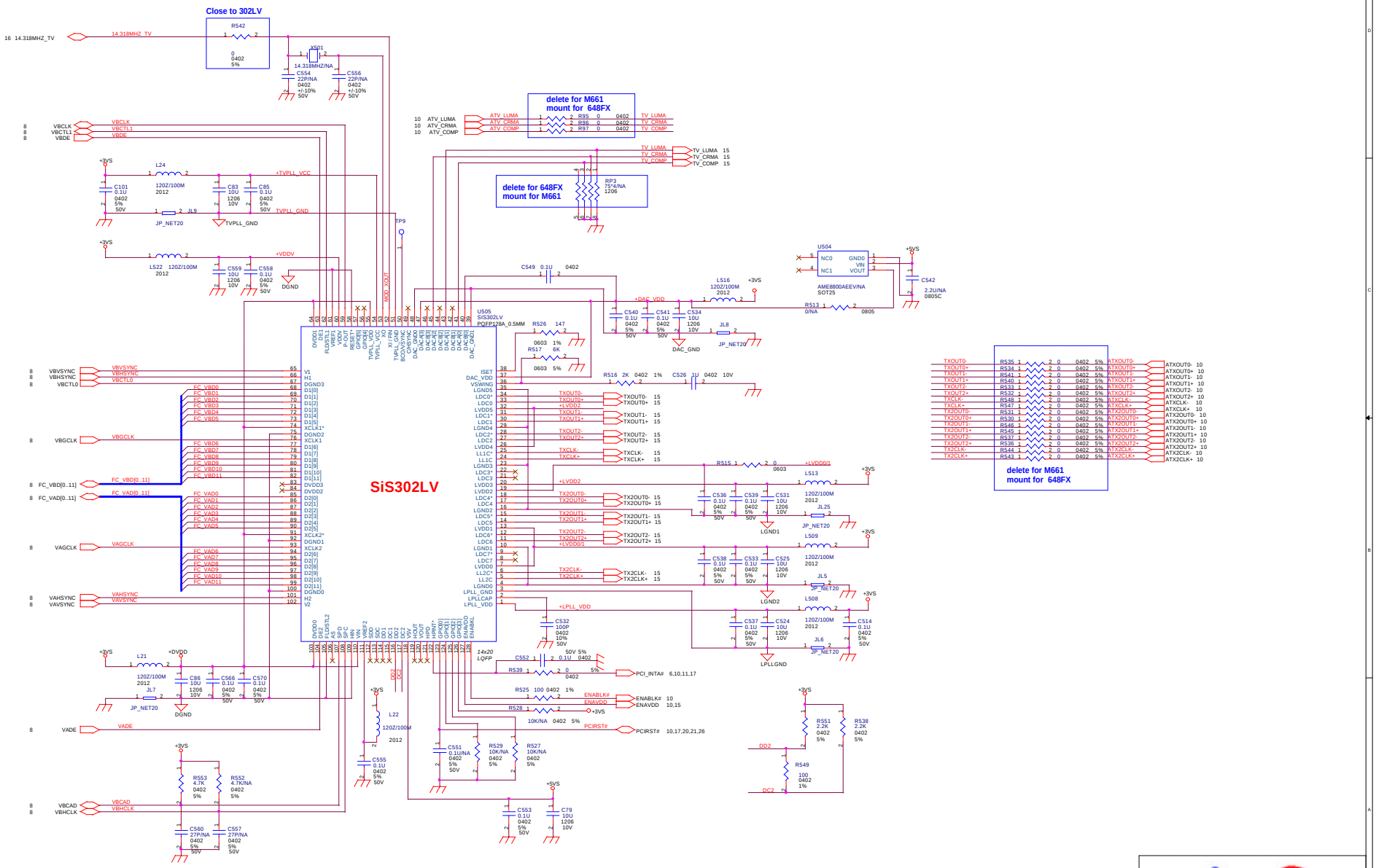
TV/LVDS ENCODER (SIS302LV)



Title	TV/LVDS ENCODER (SIS302LV)		
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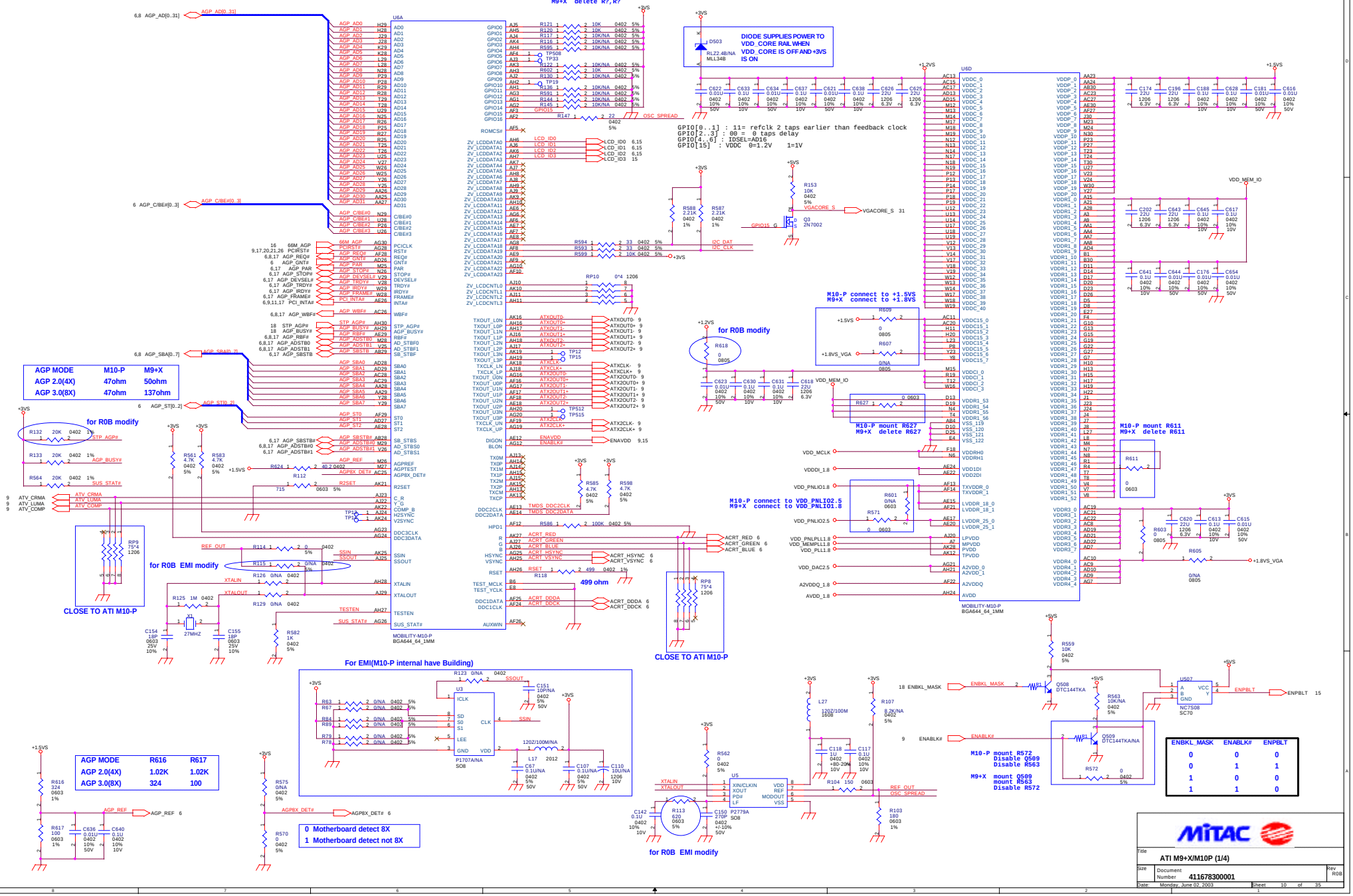
ATI M9+X/M10P (1/4)



Title	ATI M9+X/M10P (1/4)
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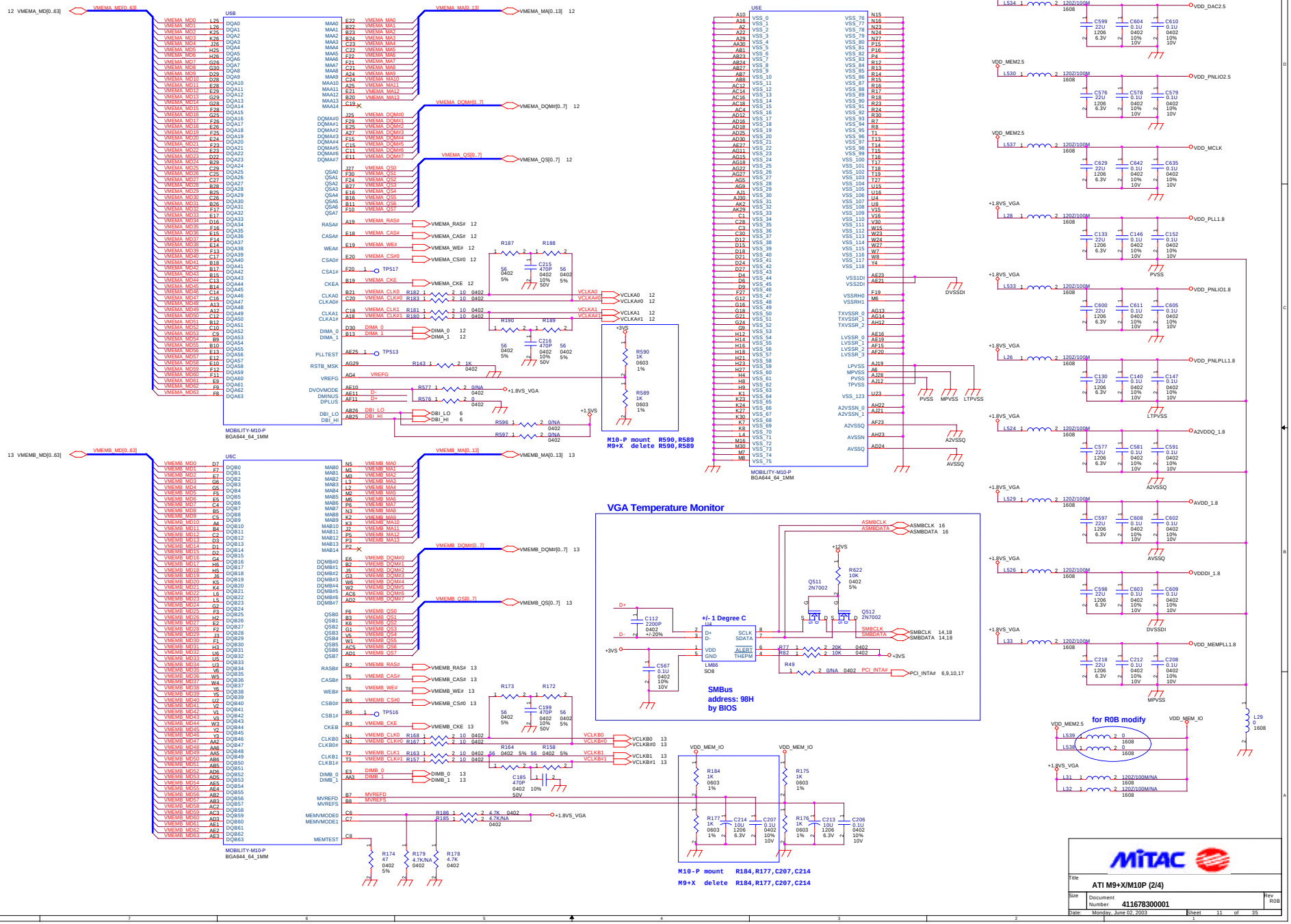
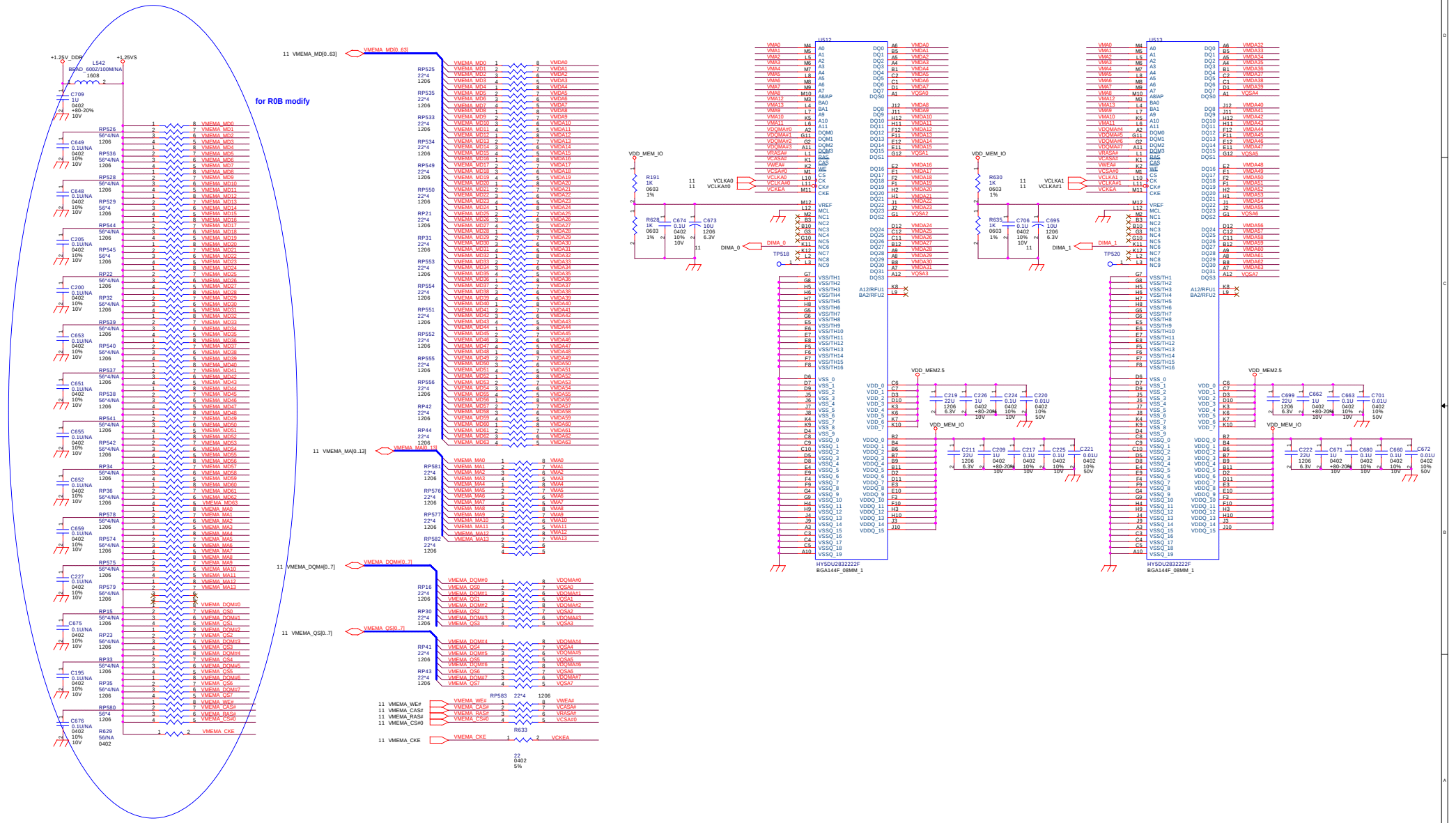
ATI M9+X/M10P (2/4)



ATI M9+X/M10P (3/4)



Title	ATI M9+X/M10P (3/4)		
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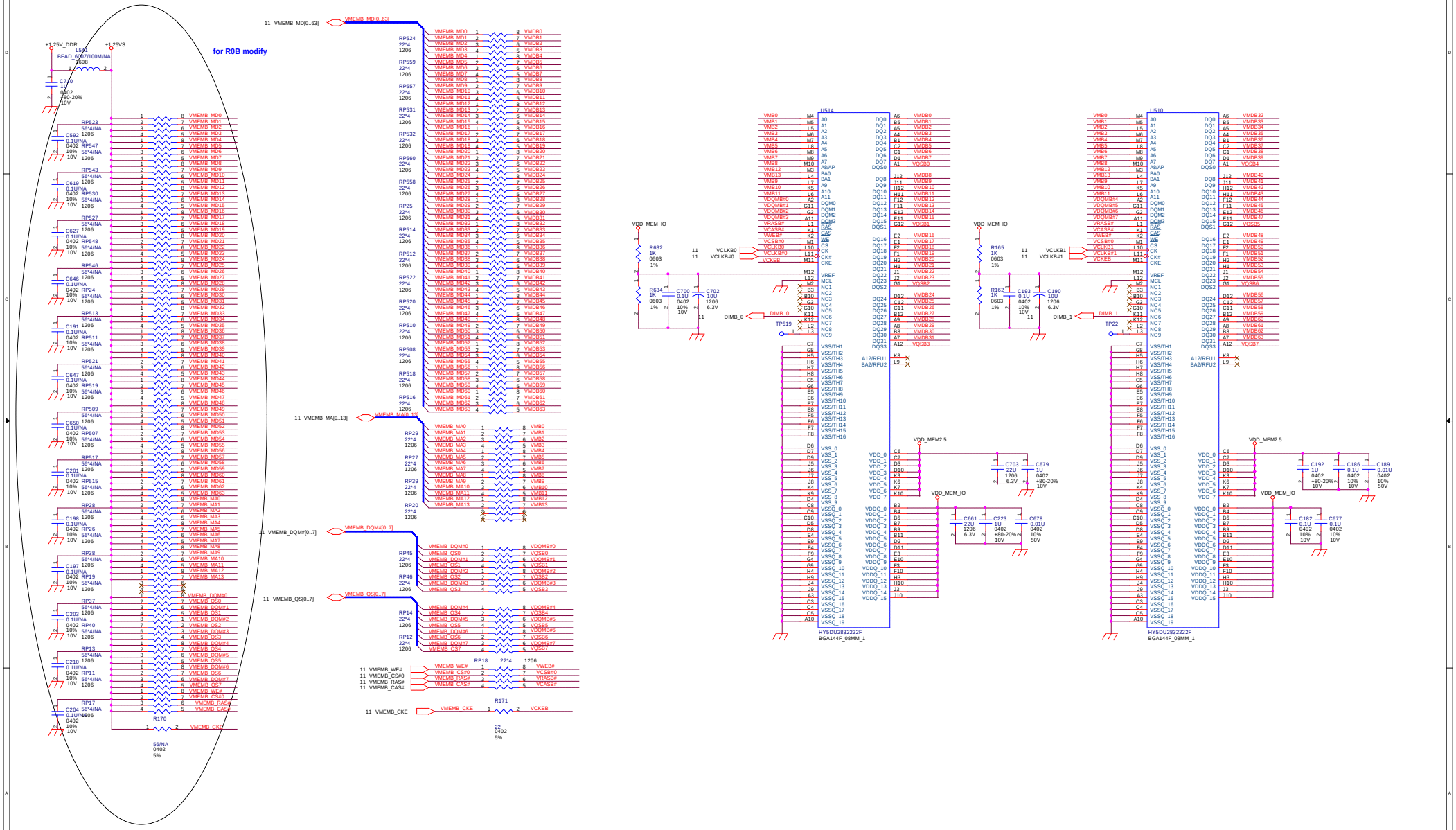
ATI M9+X/M10P (4/4)



Title	ATI M9+X/M10P (4/4)
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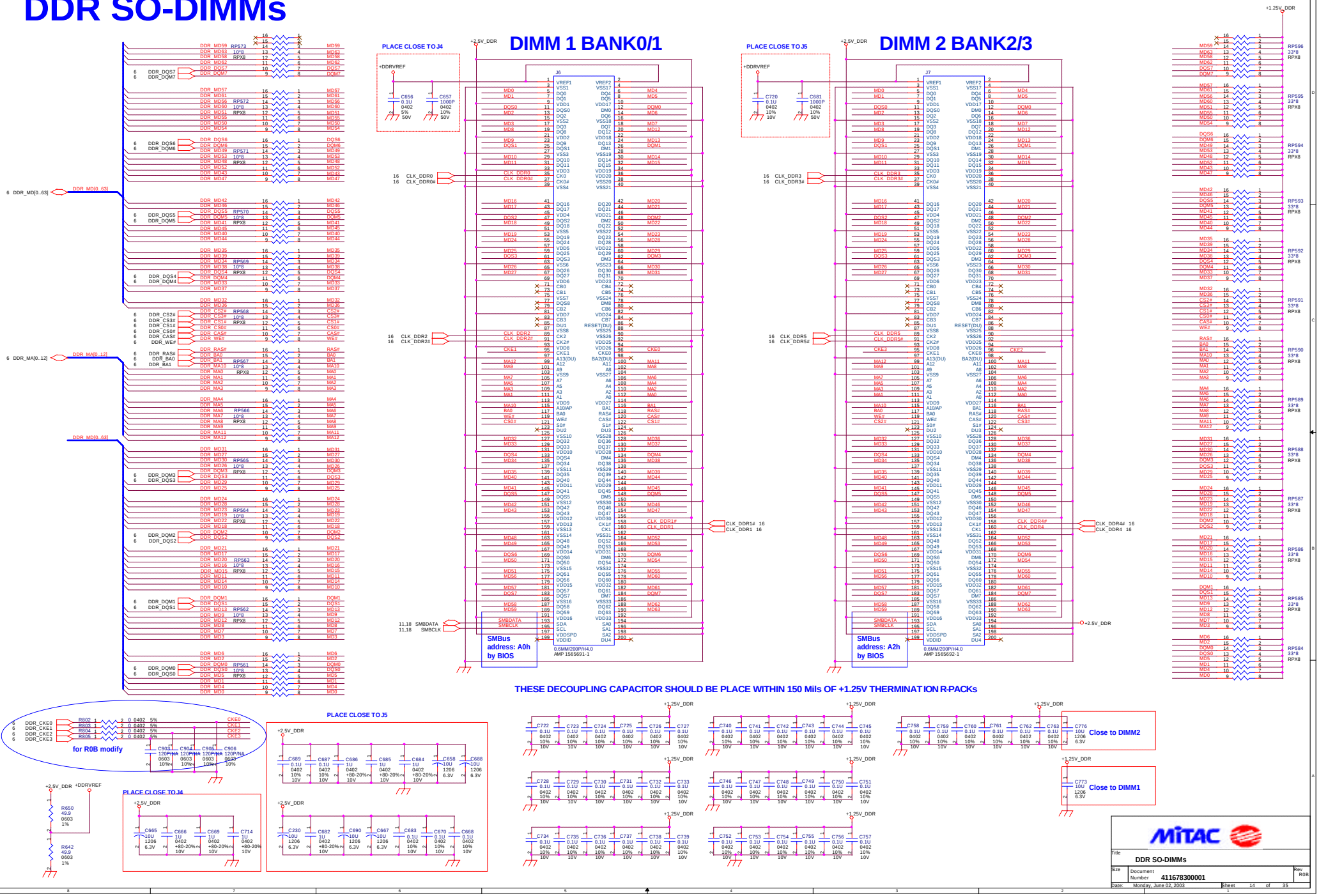
DDR SO-DIMMs


DIMM 1 BANK0/1
DIMM 2 BANK2/3
PLACE CLOSE TO J4
PLACE CLOSE TO J5
SMBus address: A0h by BIOS
SMBus address: A2h by BIOS
THESE DECOUPLING CAPACITOR SHOULD BE PLACE WITHIN 150 Mils OF +1.25V THERMINATION R-PACKs
for R0B modify
Close to DIMM2
Close to DIMM1

Title	DDR SO-DIMMs
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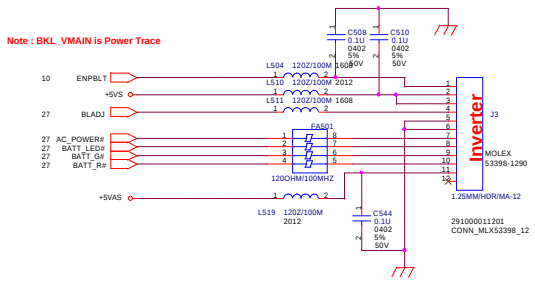
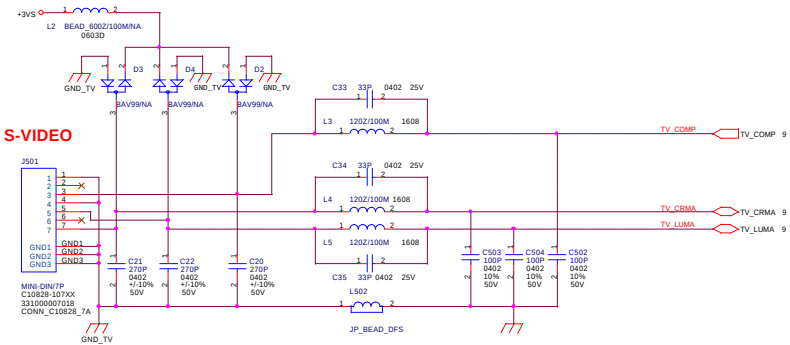
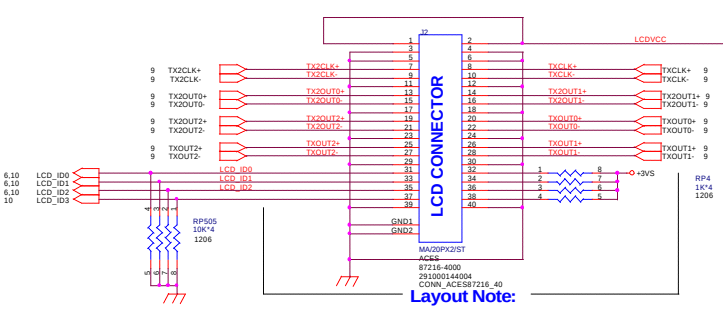
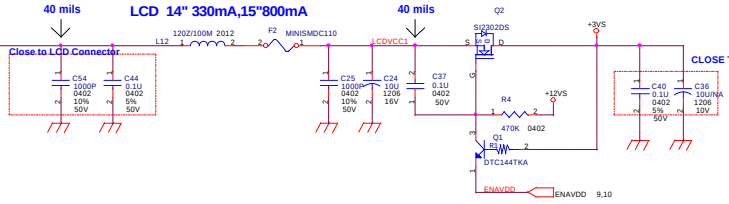
LCD / VGA INTERFACE



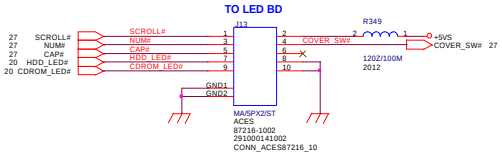






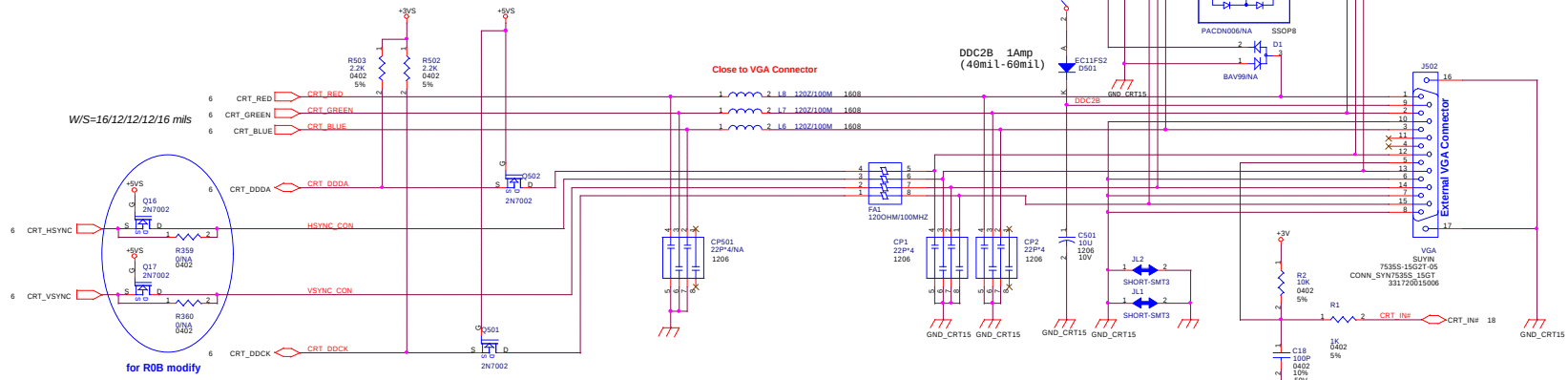
Layout Note:

S/W/W/S=12/6/6/12 mils
as short as possible
四組各自平行走線等長



LCD Panel ID

LCDID3	LCDID2	LCDID1	LCDID0	PANEL		VENDOR
0	0	0	0	X		
0	0	0	1	QDI141X1LH12	XGA	QDI
0	0	1	0	B141XN04-2	XGA	AU
0	0	1	1	N141X6-L01	XGA	CHI MEI
0	1	0	0	HSD150PX11-B	XGA	HANNSTAR
0	1	0	1	HT15X31-100	XGA	HYUNDAI
0	1	1	0	B150PC01	SXGA+	AU
0	1	1	1	X		



MiTAC	Title	LCD&VGA INTERFACE
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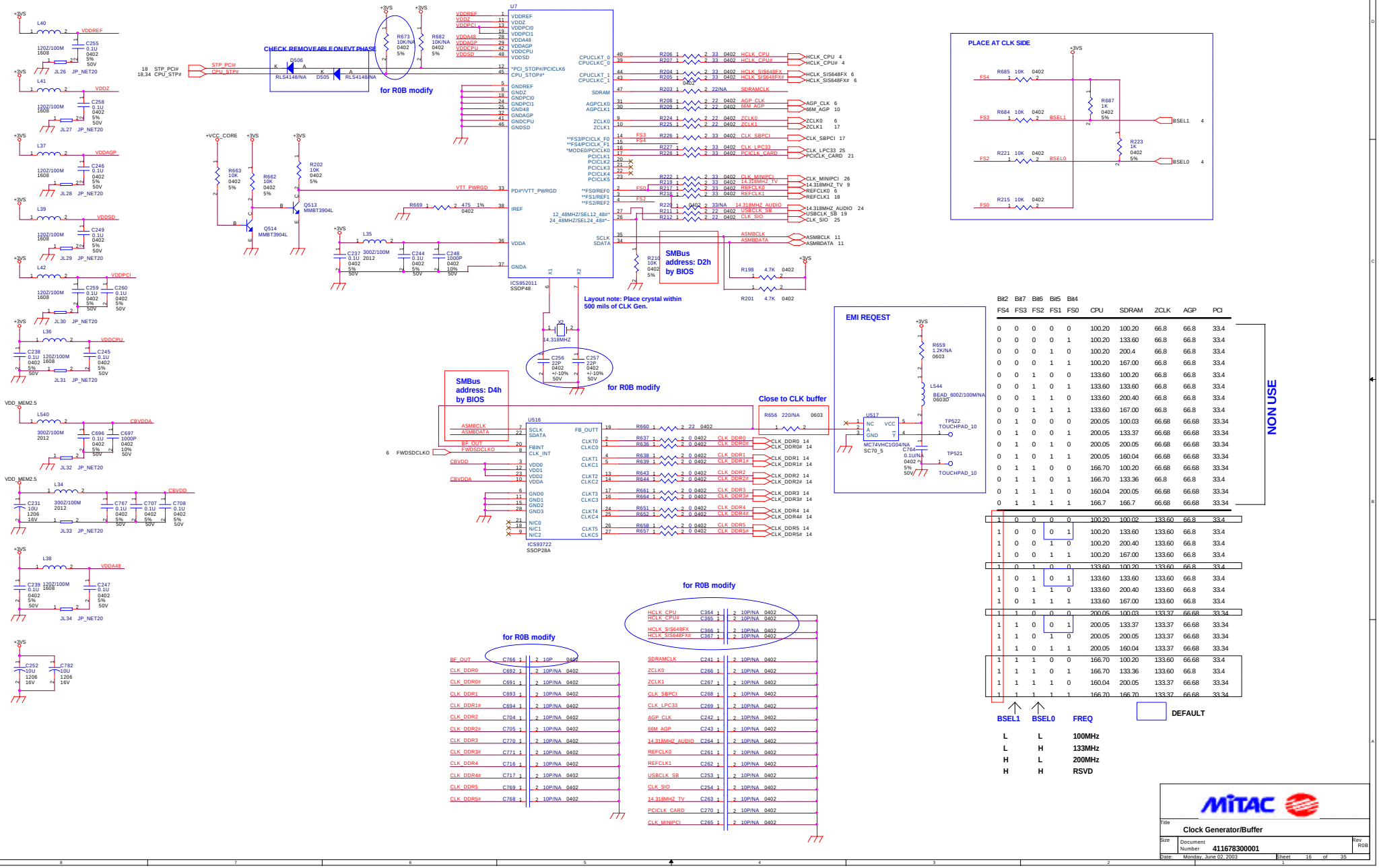
Clock Generator/Buffer

* INTERNAL PULL UP RESISTOR
** INTERNAL PULL DOWN RESISTOR
~ THIS OUTPUT HAS 1.5X DRIVE STRENGTH


CHECK REMOVEABLE ON EVT PHASE
for R0B modify
SMBus address: D2h by BIOS
SMBus address: D4h by BIOS
Layout note: Place crystal within 500 mils of CLK Gen.
Close to CLK buffer
EMI REQEST
PLACE AT CLK SIDE
NON USE
DEFAULT

Bit2 FS4	Bit7 FS3	Bit6 FS2	Bit5 FS1	Bit4 FS0	CPU	SDRAM	ZCLK	AGP	PCI
0	0	0	0	0	100.20	100.20	66.8	66.8	33.4
0	0	0	0	1	100.20	133.60	66.8	66.8	33.4
0	0	0	1	0	100.20	200.4	66.8	66.8	33.4
0	0	0	1	1	100.20	167.00	66.8	66.8	33.4
0	0	1	0	0	133.60	100.20	66.8	66.8	33.4
0	0	1	0	1	133.60	133.60	66.8	66.8	33.4
0	0	1	1	0	133.60	200.40	66.8	66.8	33.4
0	0	1	1	1	133.60	167.00	66.8	66.8	33.4
0	1	0	0	0	200.05	100.03	66.68	66.68	33.34
0	1	0	0	1	200.05	133.37	66.68	66.68	33.34
0	1	0	1	0	200.05	200.05	66.68	66.68	33.34
0	1	0	1	1	200.05	160.04	66.68	66.68	33.34
0	1	1	0	0	166.70	100.20	66.68	66.68	33.34
0	1	1	0	1	166.70	133.36	66.8	66.8	33.4
0	1	1	1	0	160.04	200.05	66.68	66.68	33.34
0	1	1	1	1	166.7	166.7	66.68	66.68	33.34
1	0	0	0	0	100.20	100.02	133.60	66.8	33.4
1	0	0	0	1	100.20	133.60	133.60	66.8	33.4
1	0	0	1	0	100.20	200.40	133.60	66.8	33.4
1	0	0	1	1	100.20	167.00	133.60	66.8	33.4
1	0	1	0	0	133.60	100.20	133.60	66.8	33.4
1	0	1	0	1	133.60	133.60	133.60	66.8	33.4
1	0	1	1	0	133.60	200.40	133.60	66.8	33.4
1	0	1	1	1	133.60	167.00	133.60	66.8	33.4
1	1	0	0	0	200.05	100.03	133.37	66.68	33.34
1	1	0	0	1	200.05	133.37	133.37	66.68	33.34
1	1	0	1	0	200.05	200.05	133.37	66.68	33.34
1	1	0	1	1	200.05	160.04	133.37	66.68	33.34
1	1	1	0	0	166.70	100.20	133.60	66.68	33.4
1	1	1	0	1	166.70	133.36	133.60	66.8	33.4
1	1	1	1	0	160.04	200.05	133.37	66.68	33.34
1	1	1	1	1	166.70	166.70	133.37	66.68	33.34

BSEL1	BSEL0	FREQ
L	L	100MHz
L	H	133MHz
H	L	200MHz
H	H	RSVD

MiTAC

Title	Clock Generator/Buffer	
Size	Document Number 411678300001	Rev R0B
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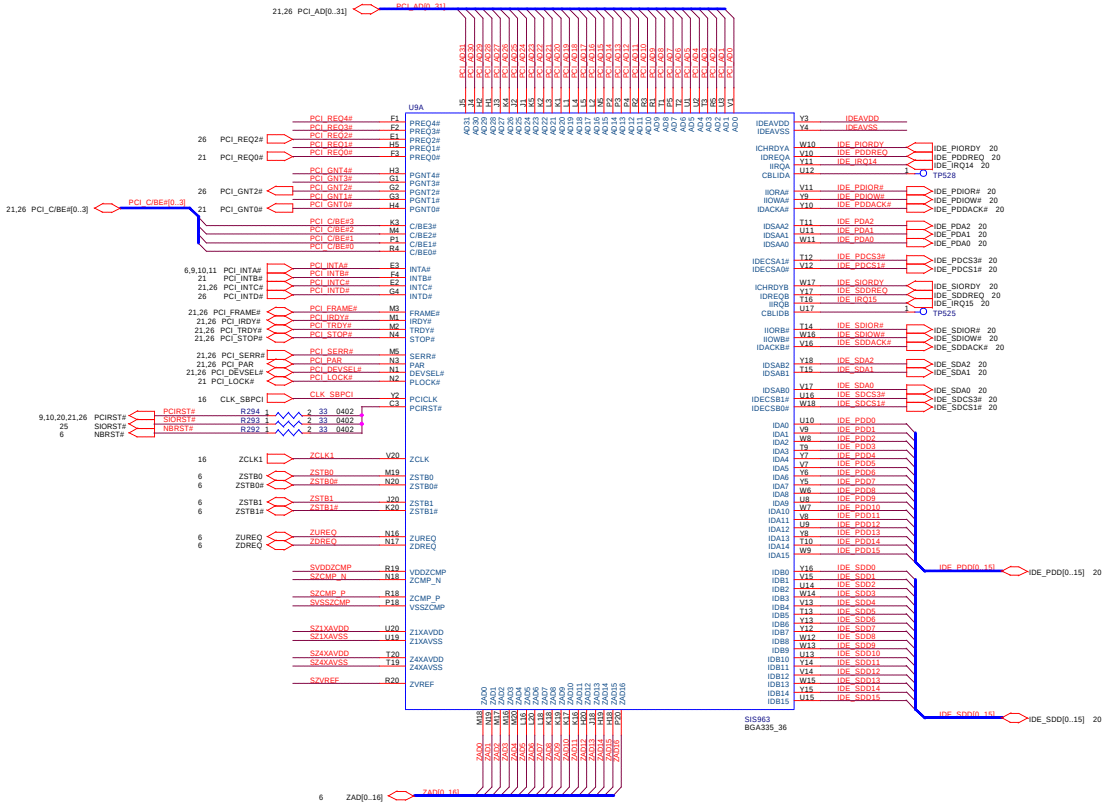
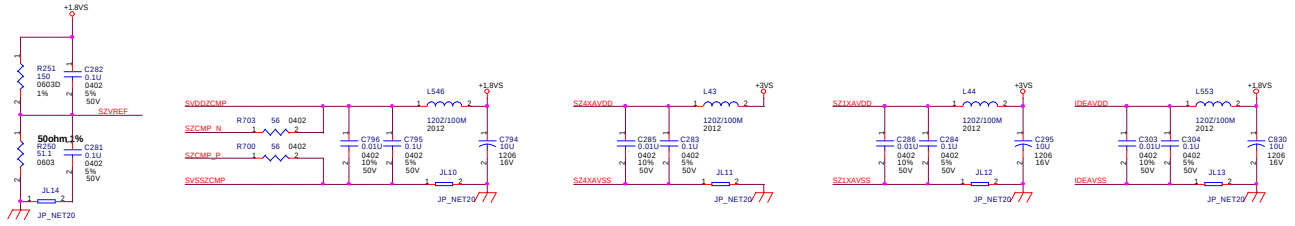
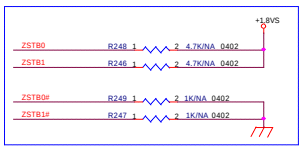
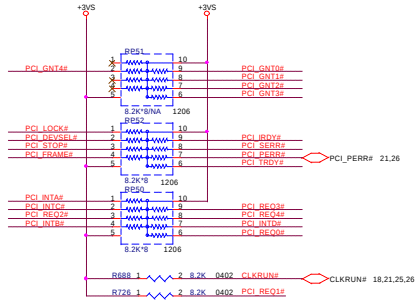
SIS963(1/3)



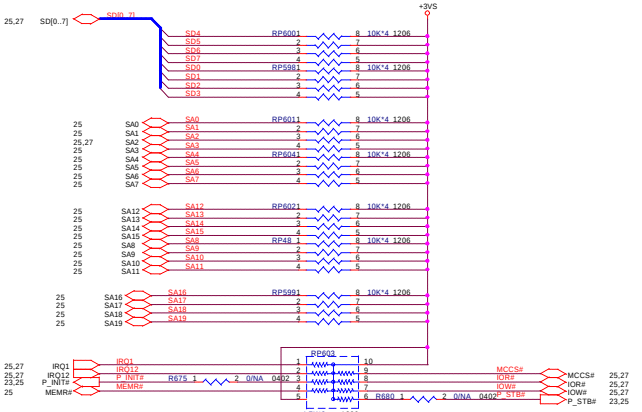




PCI BUS PULL UP RESISTERS

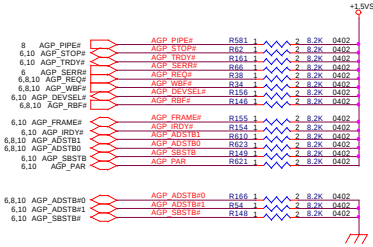


ISA BUS PULL UP RESISTERS



AGP BUS PULL UP/DOWN RESISTORS

FOR 648FX ONLY



MiTAC

Title	SIS963 (1/3)
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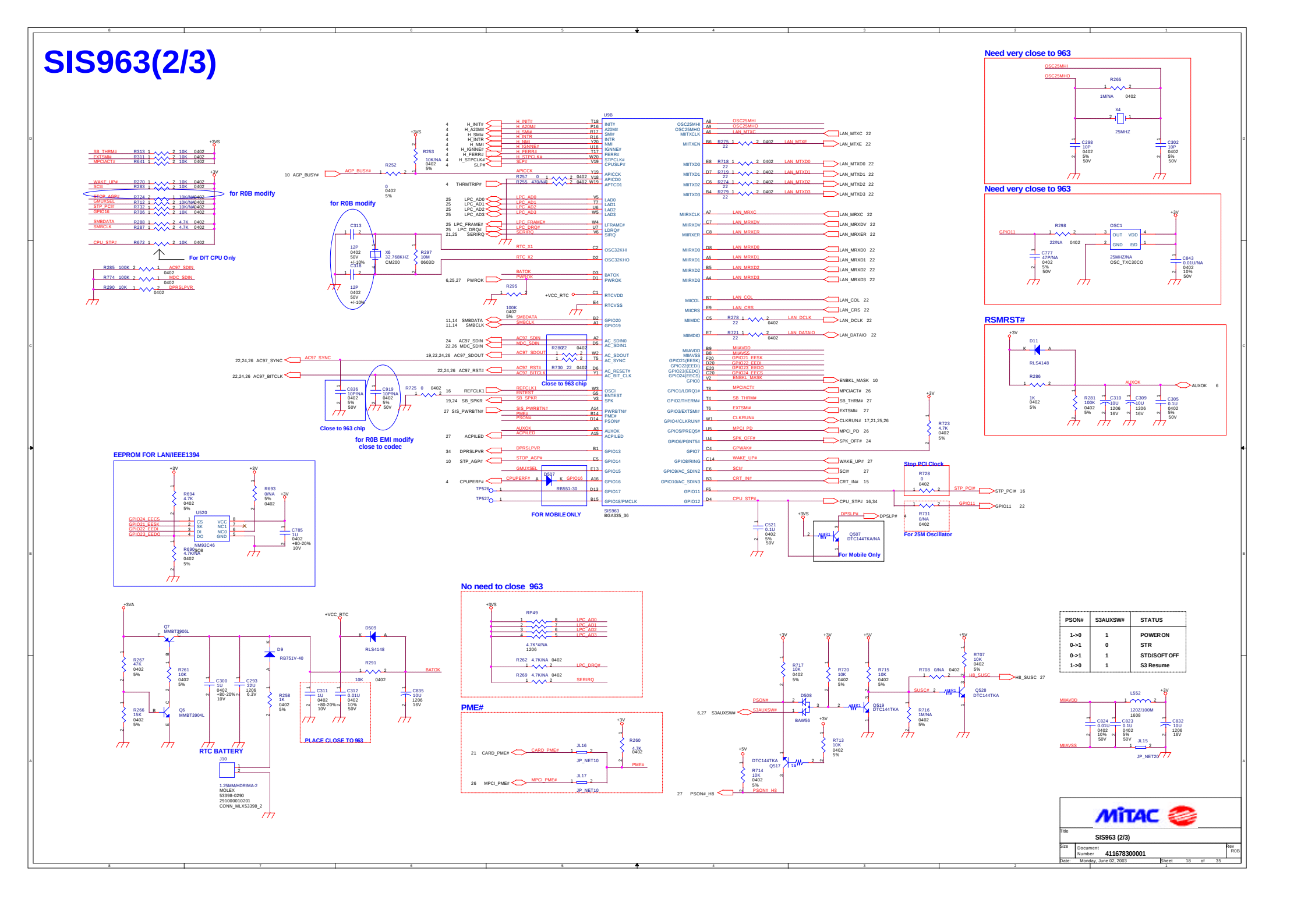
SIS963(2/3)


Need very close to 963
OSC25MHI
OSC25MHO
R265
1M/NA
0402
X4
25MHZ
C298
10P
0402
5%
50V
C302
10P
0402
5%
50V
Need very close to 963
GPIO11
R298
22/NA
0402
OSC1
OUT
VDD
GND
E/D
25MHZ/NA
OSC_TXC30CO
C777
47P/NA
0402
5%
50V
C843
0.01U/NA
0402
10%
50V
RSMRST#
+3V
D11
K
A
RLS4148
R286
1K
0402
5%
AUXOK
AUXOK 6
R281
100K
0402
5%
C310
10U
1206
16V
C309
10U
1206
16V
C305
0.1U
0402
5%
50V
SB_THRM# R313 10K 0402
EXTSMI# R311 10K 0402
MPCIACT# R641 10K 0402
WAKE_UP# R270 10K 0402
SCI# R283 10K 0402
for R0B modify
SYDR_AGP# R724 10K/NA 0402
GMUXSEL R712 10K/NA 0402
STP_PCI# R732 10K/NA 0402
GPIO16 R706 10K 0402
SMBDATA R288 4.7K 0402
SMBCLK R287 4.7K 0402
CPU_STP# R672 10K 0402
For D/T CPU Only
R285 100K AC97_SDIN 0402
R774 100K MDC_SDIN 0402
R290 10K DPRSLPVR 0402
U9B
H_INIT# T18
H_A20M# P16
H_SMI# R17
H_INTR R16
H_NMI Y20
H_IGNNE# U18
H_FERR# T17
H_STPCLK# W20
SLP# V19
APICCK V19
APICCD V18
APTCD1 W19
LAD0 V5
LAD1 T7
LAD2 U6
LAD3 W5
LFRAME# W4
LDRQ# U7
SIRQ V6
RTC_X1 C2
RTC_X2 D2
OSC32KHI
OSC32KHO
BATOK D3
PWROK D1
RTCVDD C1
RTCVSS E4
GPIO20 B2
GPIO19 A1
AC_SDIN0 A2
AC_SDIN1 D5
AC_SDOUT W2
AC_SYNC T5
AC_RESET# D6
AC_BIT_CLK Y1
OSCI W3
ENTEST G5
SPK V3
PWRBTN# A14
PME# B14
PSON# D14
AUXOK A3
ACPILED A15
GPIO13 B1
GPIO14 E5
GPIO15 E13
GPIO16 A16
GPIO17 D13
GPIO18/PMCLK B15
SIS963 BGA335_36
for R0B modify
X6 32.768KHZ CM200
R297 10M 0603D
C313 12P 0402 50V +/-10%
C318 12P 0402 50V +/-10%
R295 100K 0402 5%
R253 10K/NA 0402 5%
R252 0 0402 5%
R257 0 R255 470/NA
Close to 963 chip
C836 10P/NA 0402 5%
C919 10P/NA 0402 5%
R725 0 0402
Close to 963 chip
for R0B EMI modify close to codec
FOR MOBILE ONLY
D507 RB551-30
TP526
TP527
LAN_MTXC 22
LAN_MTXE 22
LAN_MTXD0 22
LAN_MTXD1 22
LAN_MTXD2 22
LAN_MTXD3 22
LAN_MRXC 22
LAN_MRXDV 22
LAN_MRXER 22
LAN_MRXD0 22
LAN_MRXD1 22
LAN_MRXD2 22
LAN_MRXD3 22
LAN_COL 22
LAN_CRS 22
LAN_DCLK 22
LAN_DATAIO 22
ENBKL_MASK 10
MPCIACT# 26
SB_THRM# 27
EXTSMI# 27
CLKRUN# 17,21,25,26
MPCI_PD 26
SPK_OFF# 24
GPWAK#
WAKE_UP# 27
SCI# 27
CRT_IN# 15
CPU_STP# 16,34
Stop PCI Clock
R728 0 0402
R731 0/NA 0402
STP_PCI# 16
GPIO11 22
For 25M Oscillator
DPSLP#
Q507 DTC144TKA/NA
For Mobile Only
R723 4.7K 0402 5%
C521 0.1U 0402 5% 50V
EEPROM FOR LAN/IEEE1394
U520 NM93C46
R694 4.7K 0402 5%
R693 0/NA 5% 0402
R690 4.7K/NA 0402 5%
C785 1U 0402 +80-20% 10V
GPIO24_EECS
GPIO21_EESK
GPIO22_EEDI
GPIO23_EEDO
No need to close 963
RP19 4.7K*4/NA 1206
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
R262 4.7K/NA 0402 LPC_DRQ#
R269 4.7K/NA 0402 SERIRQ
PME#
CARD_PME# JL16 JP_NET10
MPCI_PME# JL17 JP_NET10
R260 4.7K 0402
RTC BATTERY
Q7 MMBT3906L
Q6 MMBT3904L
D9 RB751V-40
D509 RLS4148
R267 47K 0402 5%
R261 10K 0402 5%
R266 15K 0402 5%
R258 1K 0402 5%
R291 10K 0402
C300 1U 0402 +80-20% 10V
C293 22U 1206 6.3V
C311 1U 0402 +80-20% 10V
C312 0.01U 0402 10% 50V
C835 10U 1206 16V
PLACE CLOSE TO 963
J10
1.25MM/HDR/MA-2
MOLEX
53398-0290
291000010201
CONN_MLX53398_2
R717 10K 0402 5%
R720 10K 0402 5%
R715 10K 0402 5%
R708 0/NA 0402
R707 10K 0402 5%
H8_SUSC 27
SUSC# 2
Q528 DTC144TKA
D508 BAW56
Q519 DTC144TKA
R716 1M/NA 0402 5%
R713 10K 0402 5%
DTC144TKA Q517
R714 10K 0402 5%
PSON#_H8
S3AUXSW# 6,27
PSON# 27
L552 120Z/100M 1608
C824 0.01U 0402 10% 50V
C823 0.1U 0402 5% 50V
C832 10U 1206 16V
JL15 JP_NET20
MIAVDD
MIAVSS
PSON# S3AUXSW# STATUS
1->0 1 POWER ON
0->1 0 STR
0->1 1 STD/SOFT OFF
1->0 1 S3 Resume
MiTAC
Title
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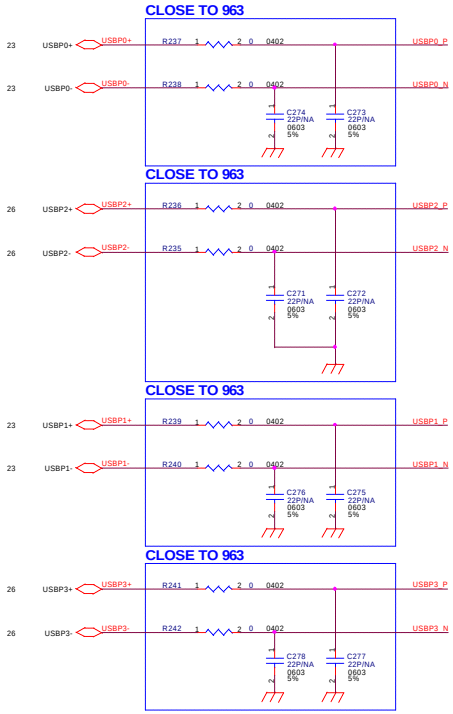
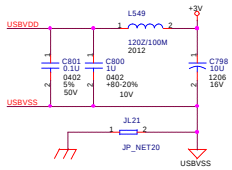
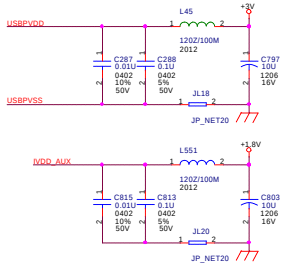
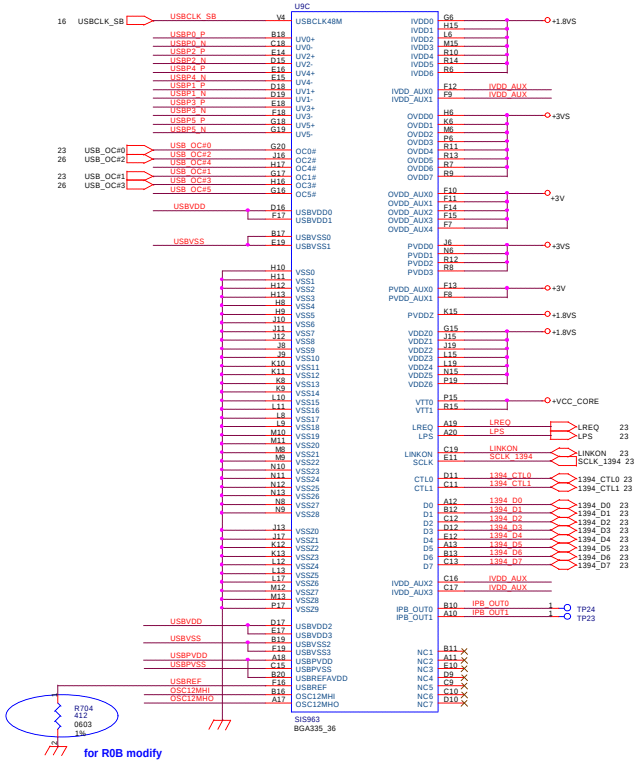
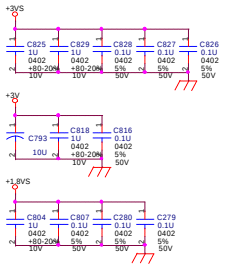
SIS963(3/3)



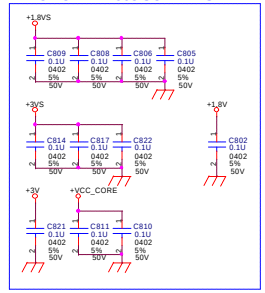




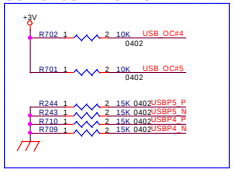




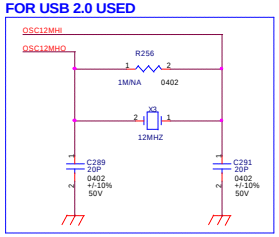
PLACE UNDER 963 SOLDER SIDE



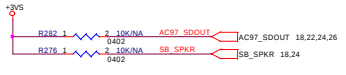
USB UNUSED PORTS



FOR USB 2.0 USED



Hardware Strap



Symbol	0	1	Default	Notes
SB_SPKR (LPC addr mapping)	disable	enable	0	Internal Pull-down
AC97_SDOUT (Trap mode)	ROM	Reserved	0	Internal Pull-down
USB_OC4# (South bridge debug mode)	enable	disable	1	
IPB_OUT0(MuTIOL clock PLL)	enable	disable	0	Internal Pull-down
IPB_OUT1(MuTIOL operation mode select)	Full-swing	Partial-swing	0	Internal Pull-down
AC97_SYNC (PCICLK PLL)	enable	disable	0	Internal Pull-down

MiTAC

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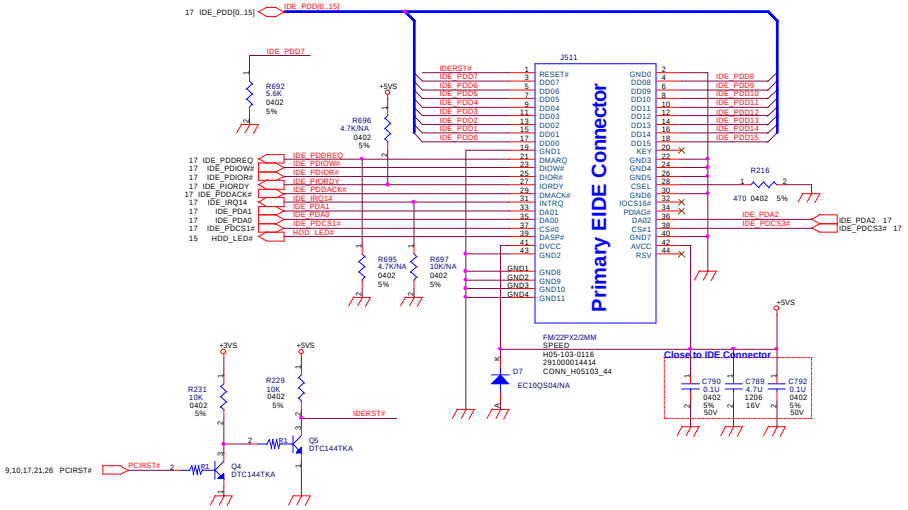
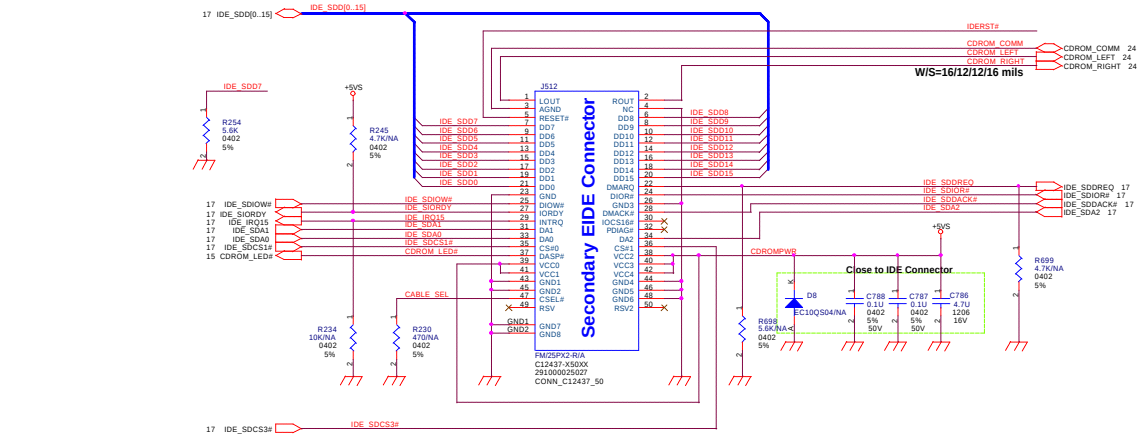
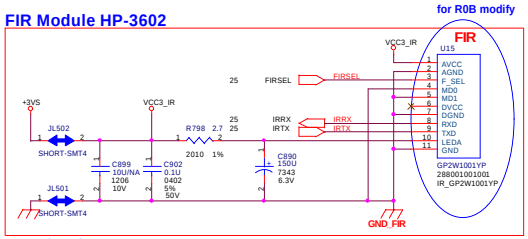
IDE INTERFACE & IR





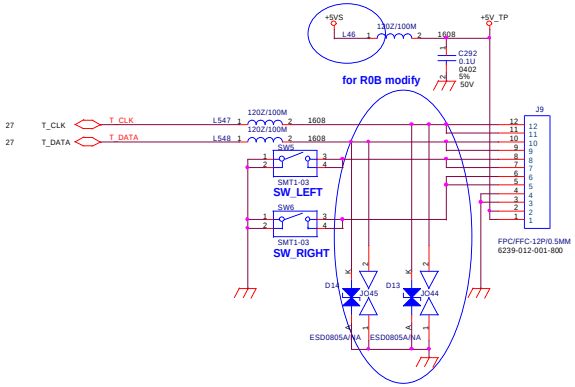
FIR Module HP-3602

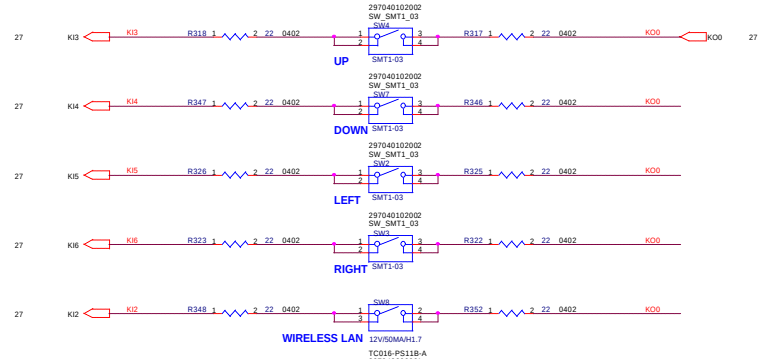
for R0B modify



IR Mode Select

IRMODE0	IRMODE1	FIRSEL	RX Function	TX Function
HI	LOW	X	Shutdown	Shutdown
LOW	LOW	LOW		Full Distance Power
LOW	HI	LOW	SIR	2/3 Distance Power
HI	HI	LOW	SIR	1/3 Distance Power
LOW	LOW	HI	MIR/FIR	Full Distance Power
LOW	HI	HI	MIR/FIR	2/3 Distance Power
HI	HI	HI	MIR/FIR	1/3 Distance Power





Title	IDE INTERFACE & IR
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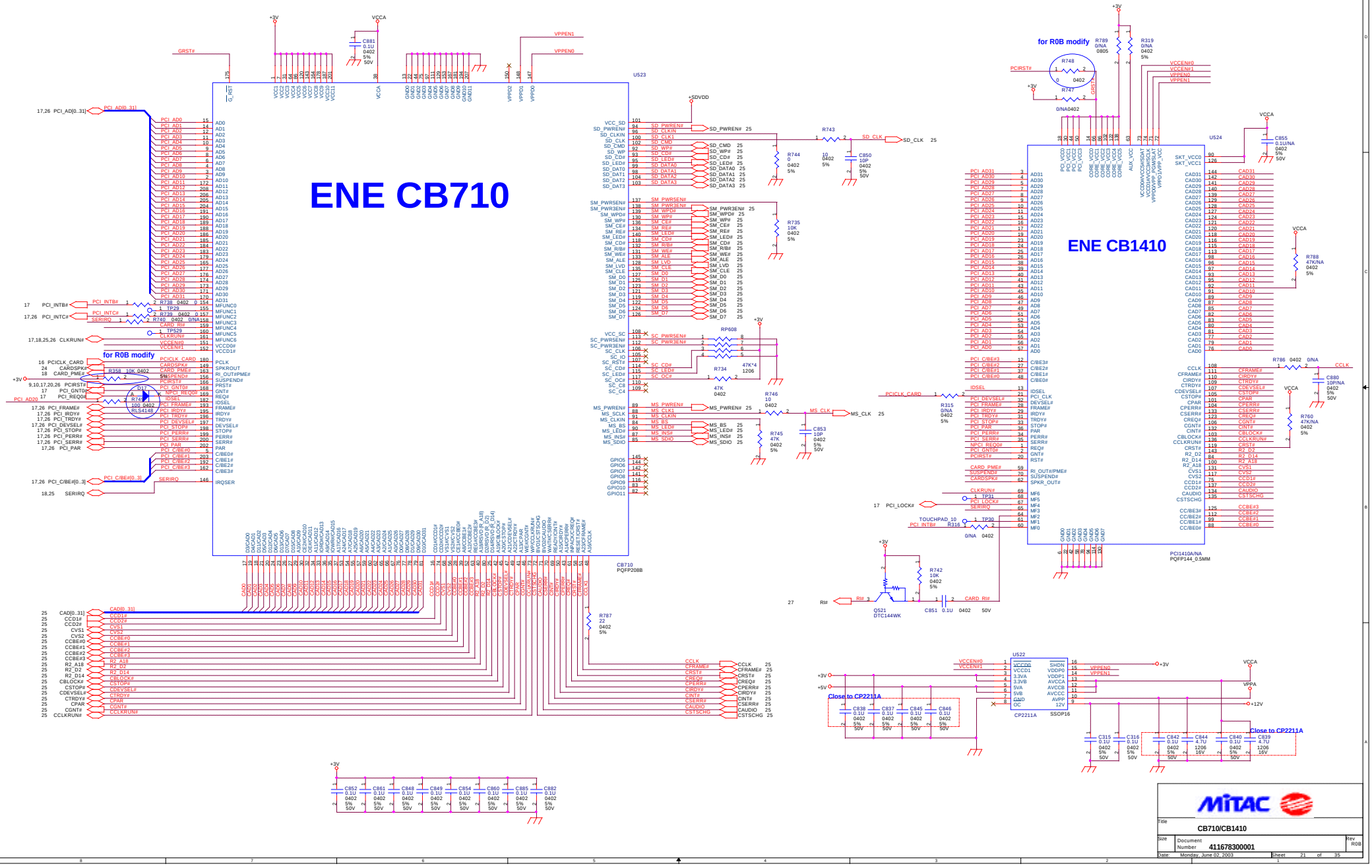
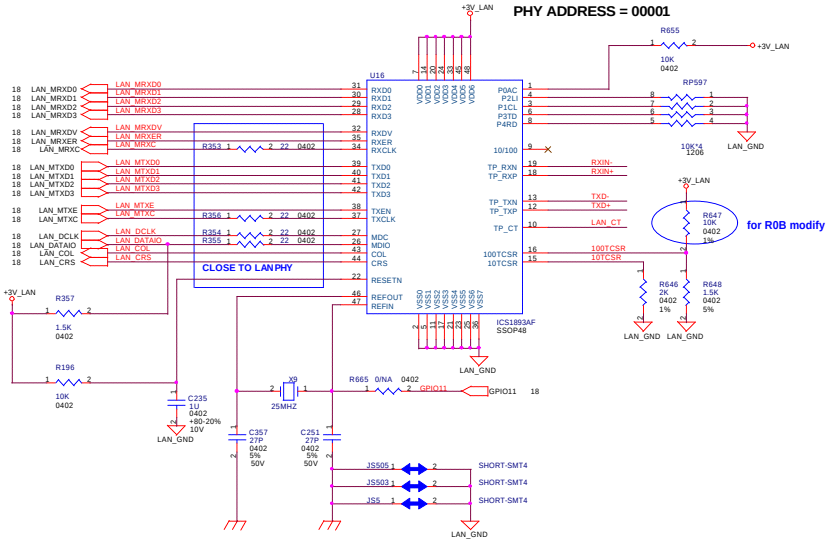
CARDBUS

ENE CB710



LAN AND MDC



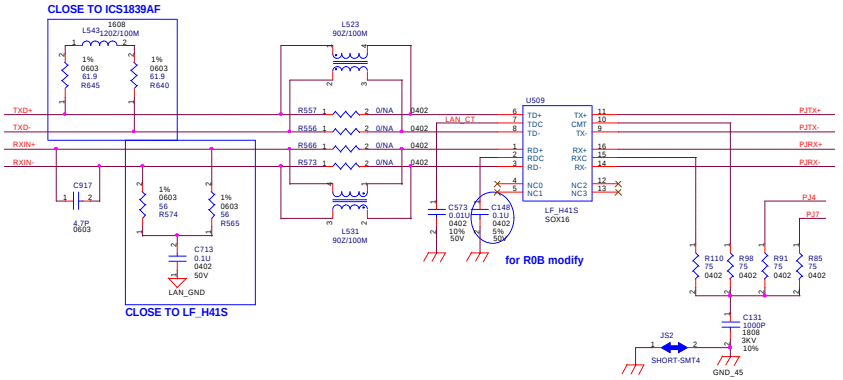
Layout Note:

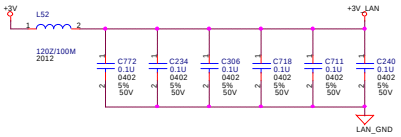
二組各自平行走線等長

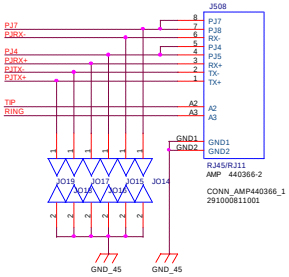
二組中間須絕緣, EX: GND

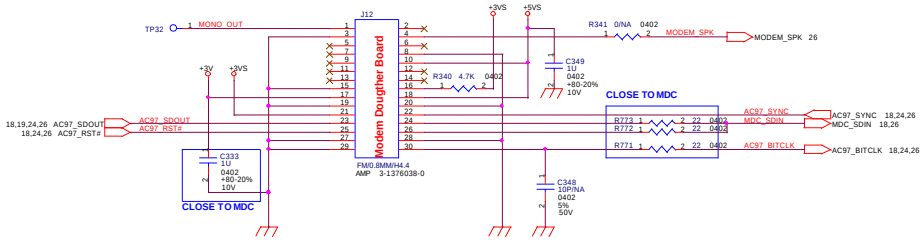
SWITCHING

as short as possible



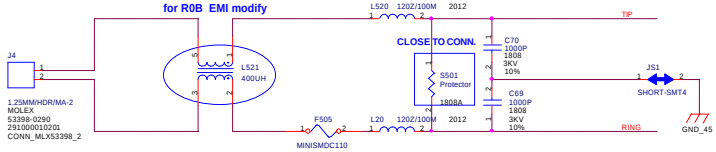






MDC HARDWARE STRAP

	HIGH	LOW
PIN 16	AUDIO CODEC ON MOTHER BD	AUDIO CODEC ON DAUGHTER BOARD



Title	LAN PHY (ICS1893AF)& MDC
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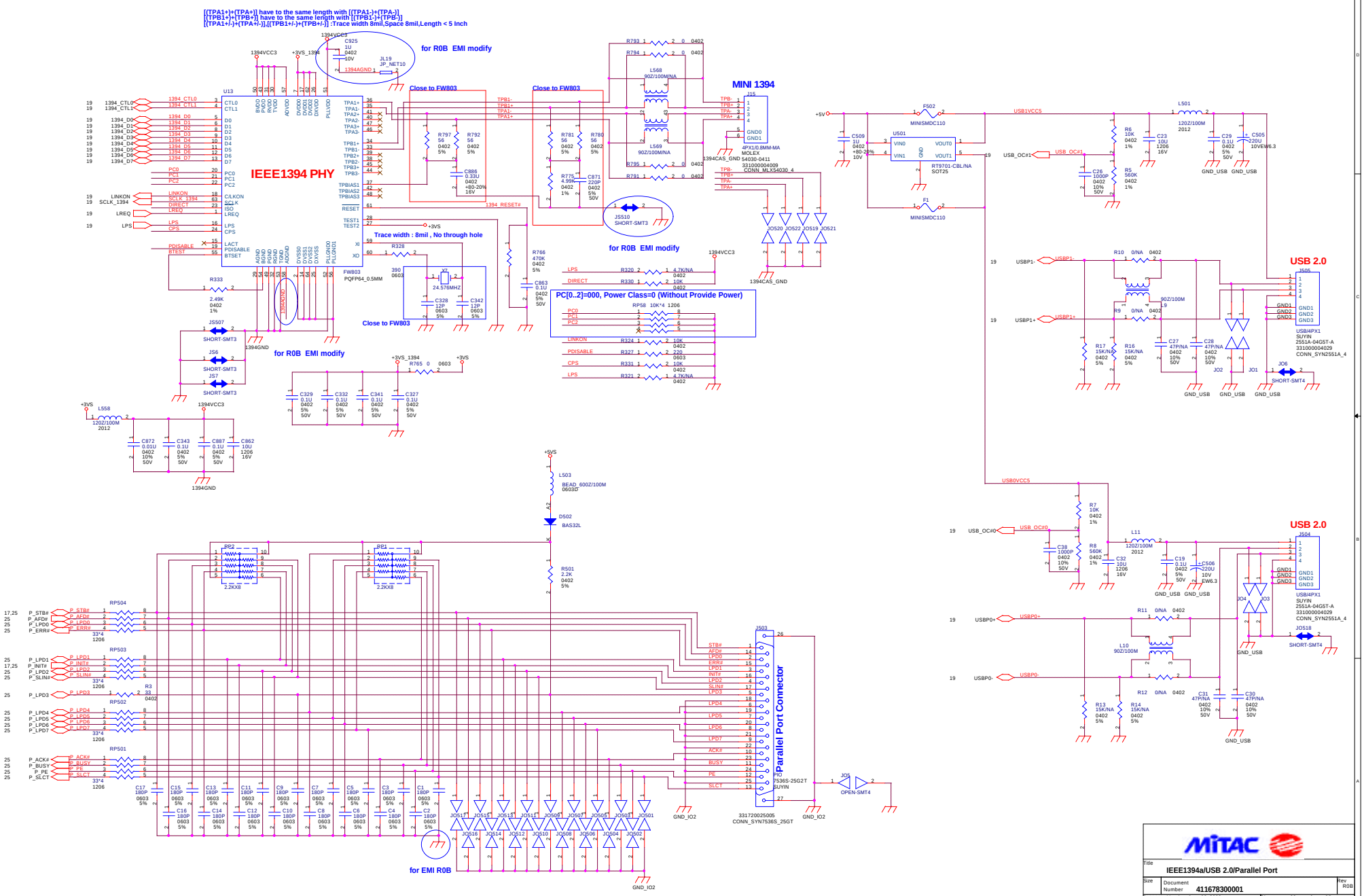
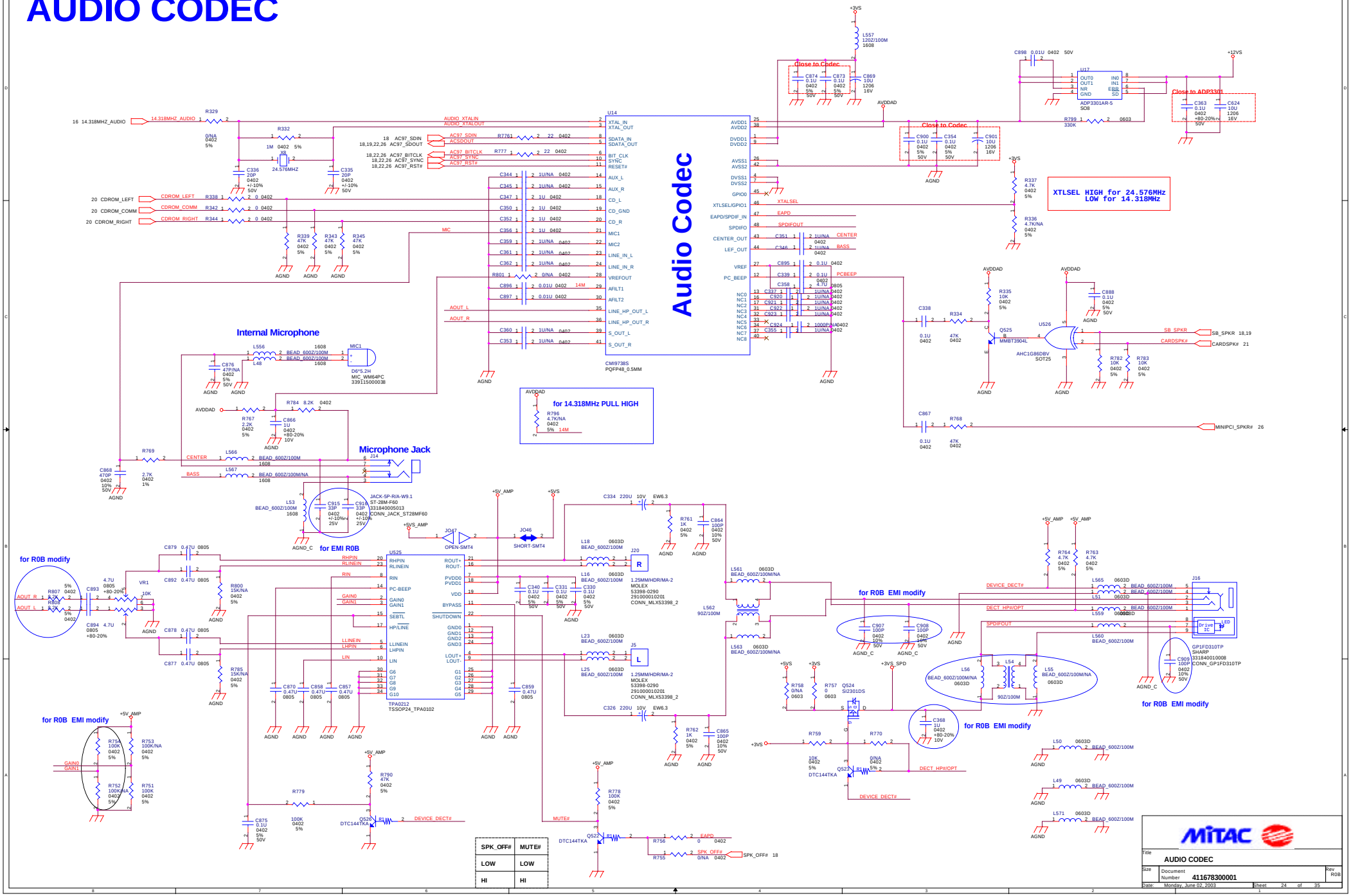
IEEE1394A/USB 2.0/Parallel Port



AUDIO CODEC


Audio Codec
CMI9738S
PQFP48_0.5MM
Internal Microphone
Microphone Jack
for 14.318MHz PULL HIGH
XTLSEL HIGH for 24.576MHz
LOW for 14.318MHz
Close to Codec
Close to ADP3301
for EMI R0B
for R0B modify
for R0B EMI modify
SPK_OFF#
MUTE#
LOW
HI
Title
AUDIO CODEC
Number
411678300001
Rev
R0B
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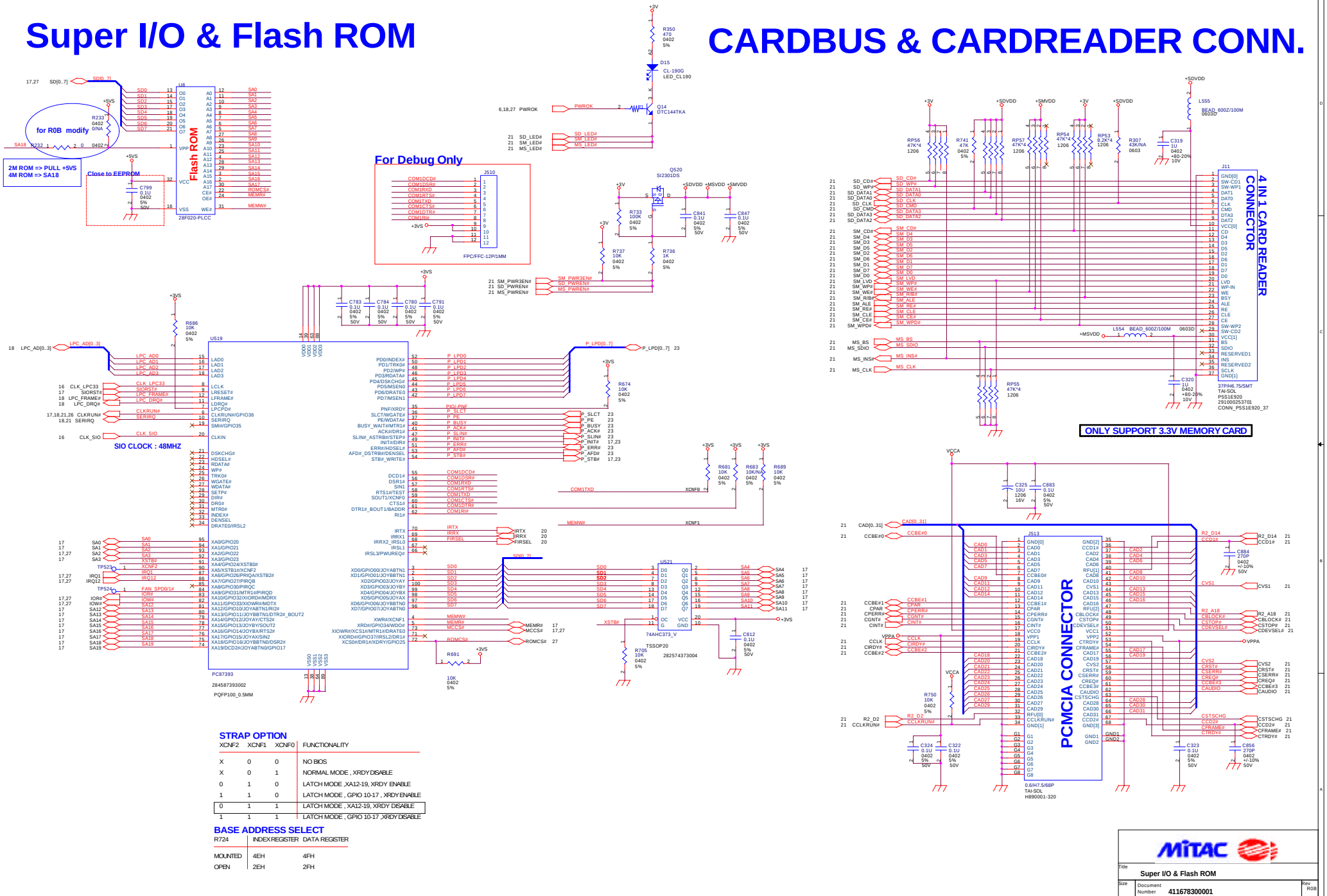
Super I/O & Flash ROM

CARDBUS & CARDREADER CONN.



STRAP OPTION

XCNF2	XCNF1	XCNF0	FUNCTIONALITY
X	0	0	NO BIOS
X	0	1	NORMAL MODE , XRDY DISABLE
0	1	0	LATCH MODE ,XA12-19, XRDY ENABLE
1	1	0	LATCH MODE , GPIO 10-17 , XRDY ENABLE
0	1	1	LATCH MODE , XA12-19, XRDY DISABLE
1	1	1	LATCH MODE , GPIO 10-17 ,XRDY DISABLE

BASE ADDRESS SELECT

R724	INDEX REGISTER	DATA REGISTER
MOUNTED	4EH	4FH
OPEN	2EH	2FH

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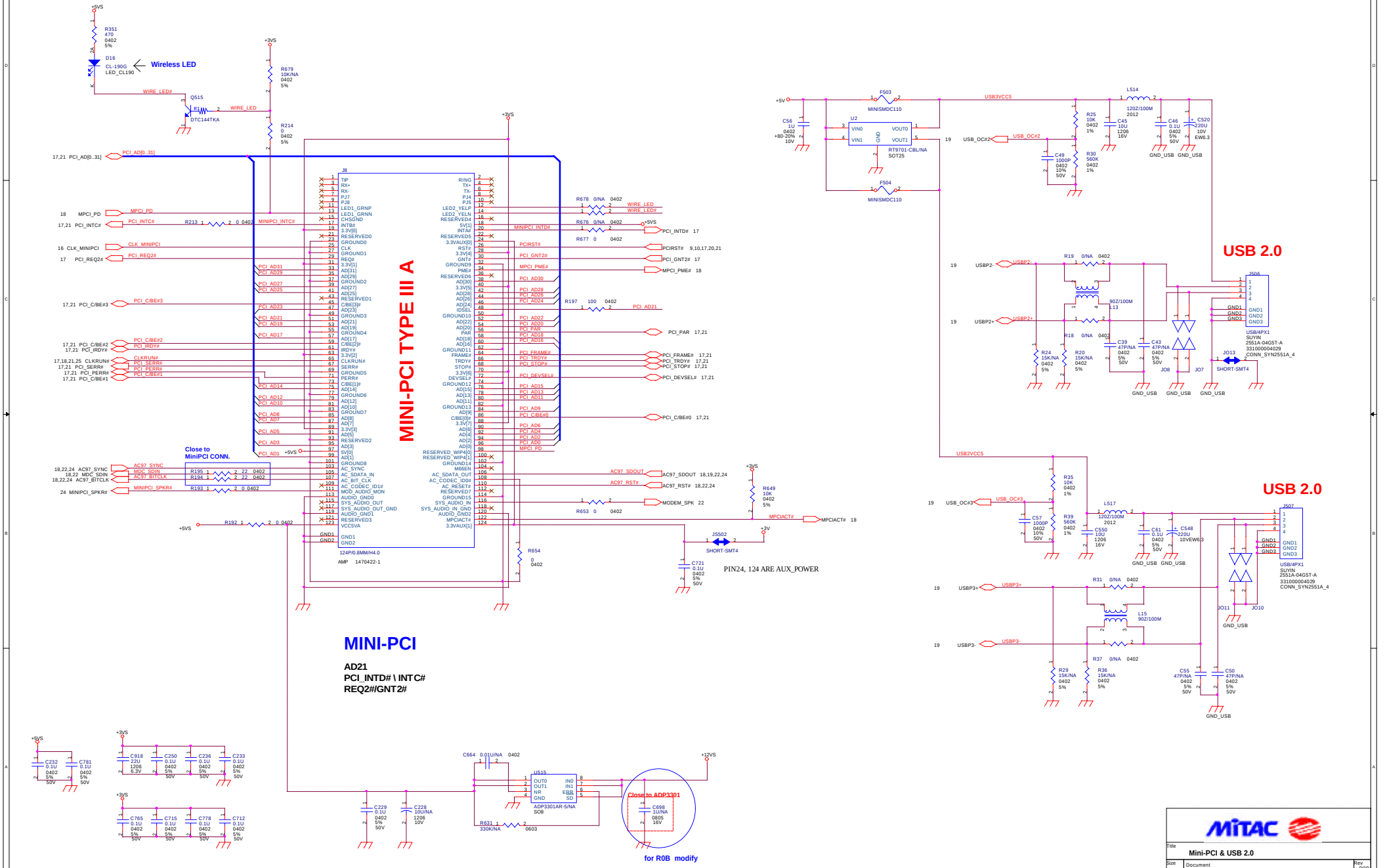
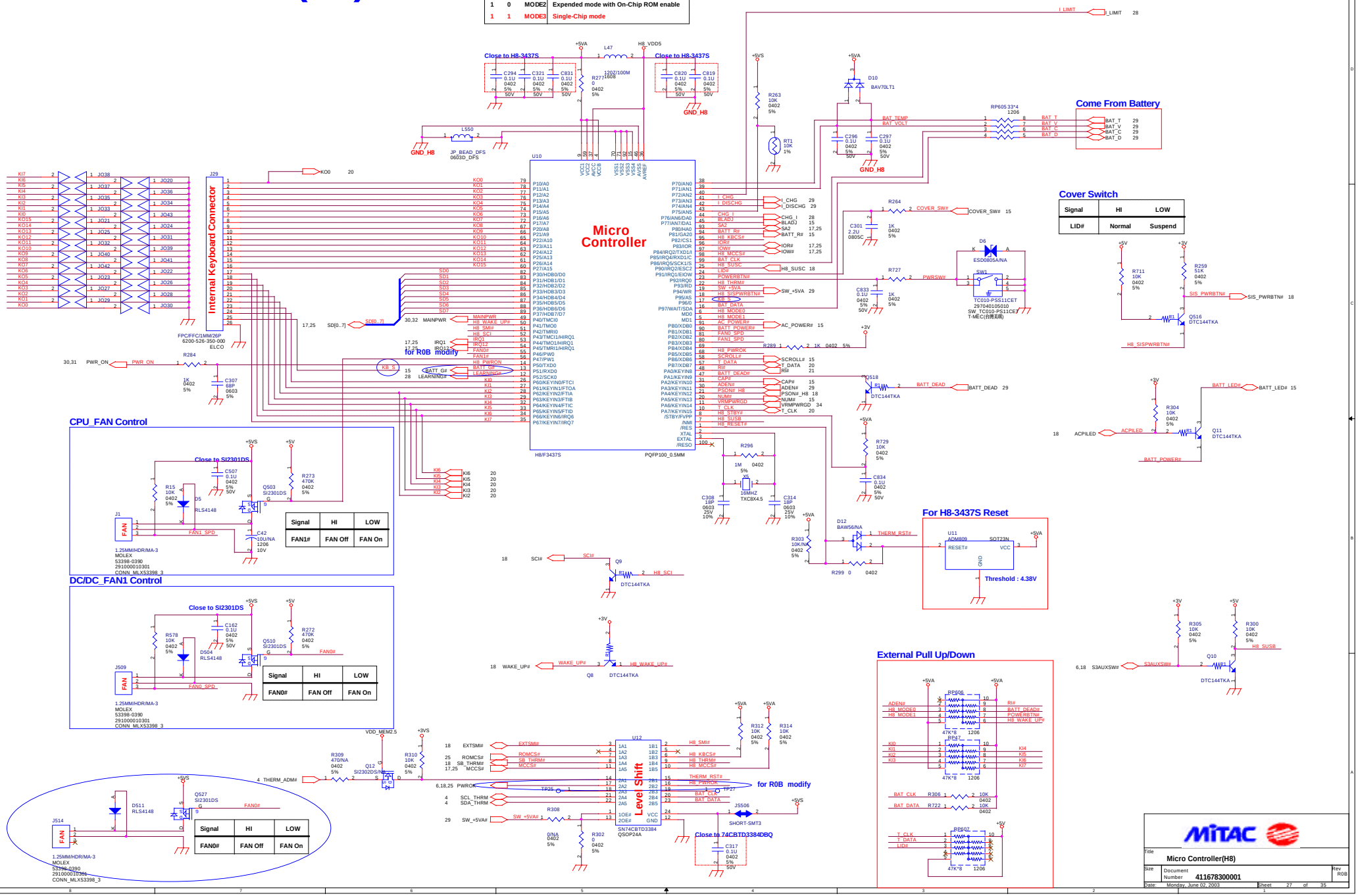
Mini-PCI & USB 2.0



Micro Controller(H8)

H8 Mode Select Table

MD0	MD1	MODE	Description
0	1	MODE1	Expended mode with On-Chip ROM disable
1	0	MODE2	Expended mode with On-Chip ROM enable
1	1	MODE3	Single-Chip mode



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Size	Document Number 411678300001 Rev R0B
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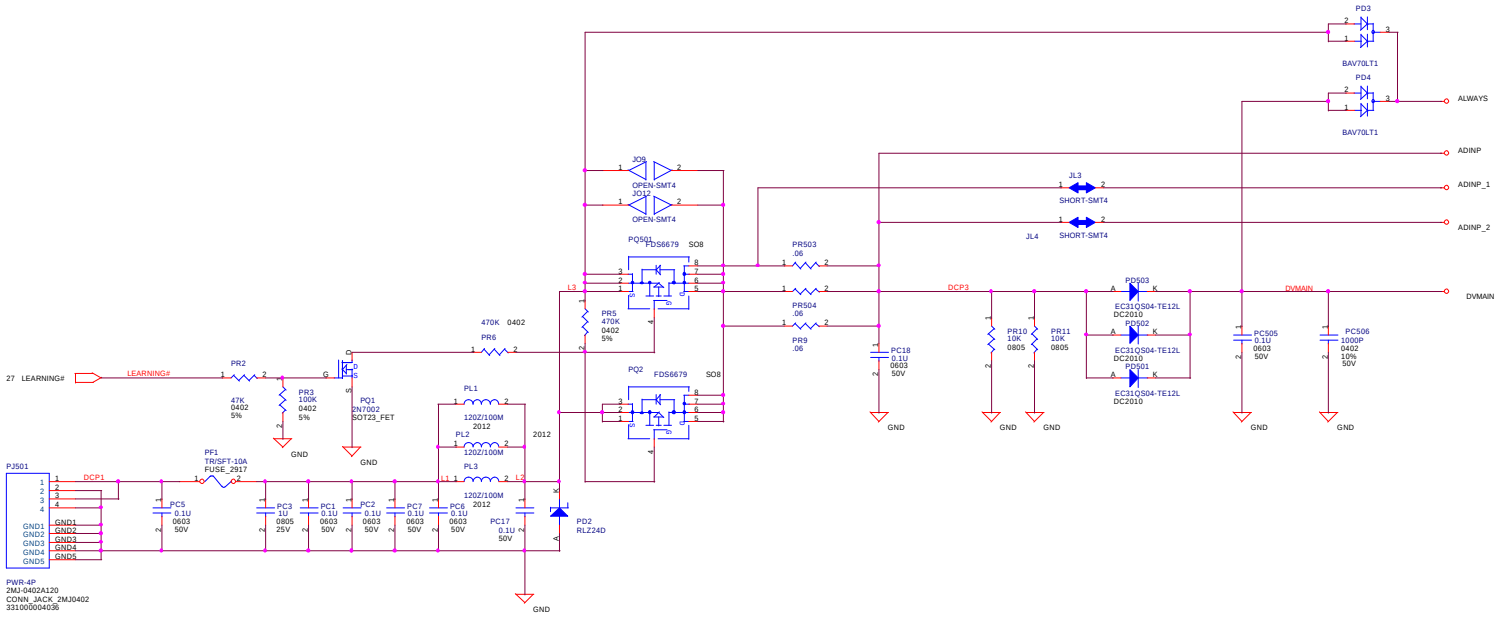

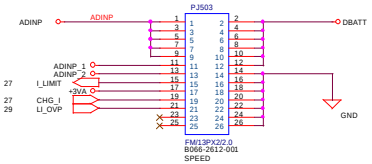

Title	DC Connector	
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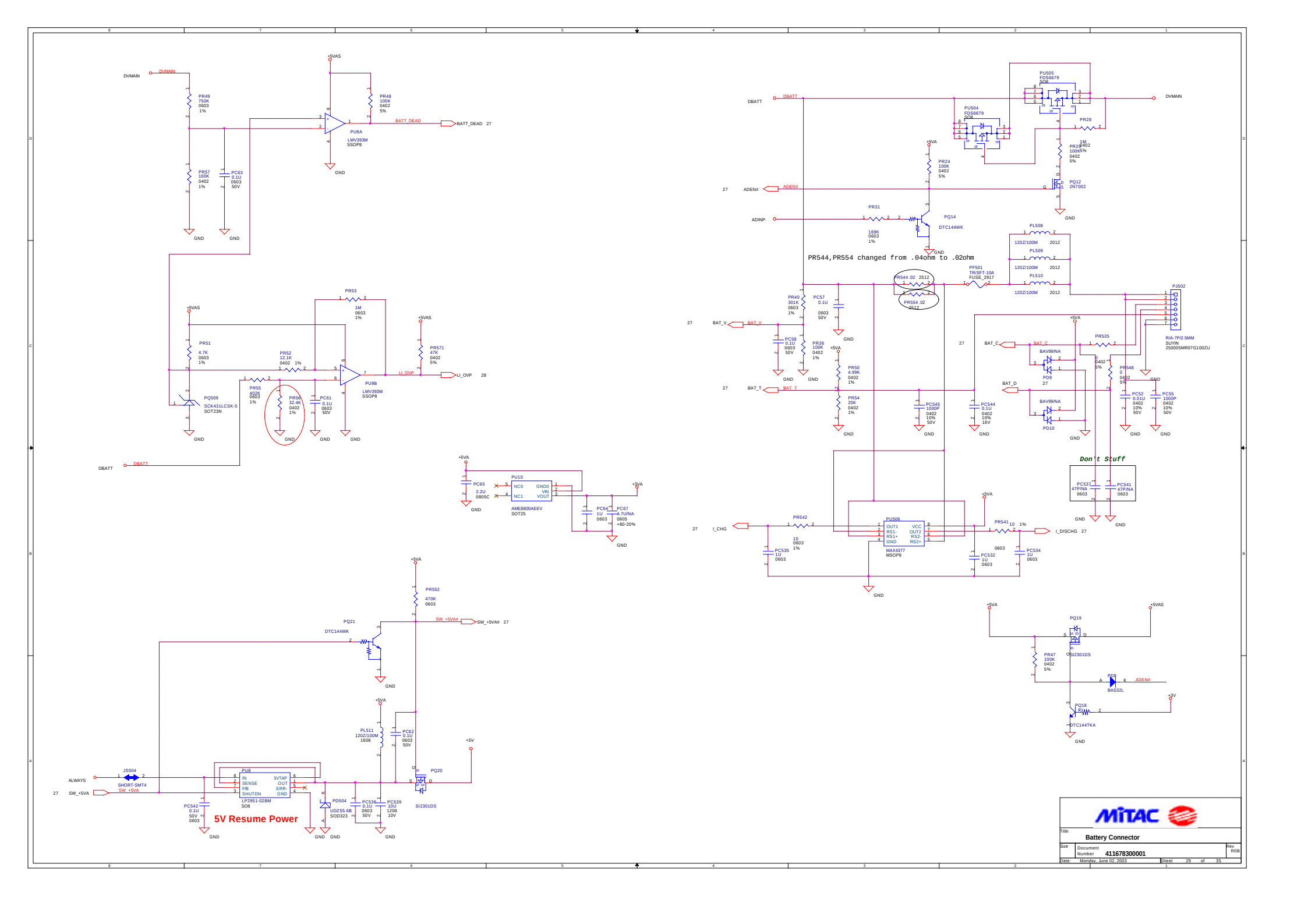
PR544,PR554 changed from .04ohm to .02ohm
Don't Stuff
5V Resume Power
Battery Connector
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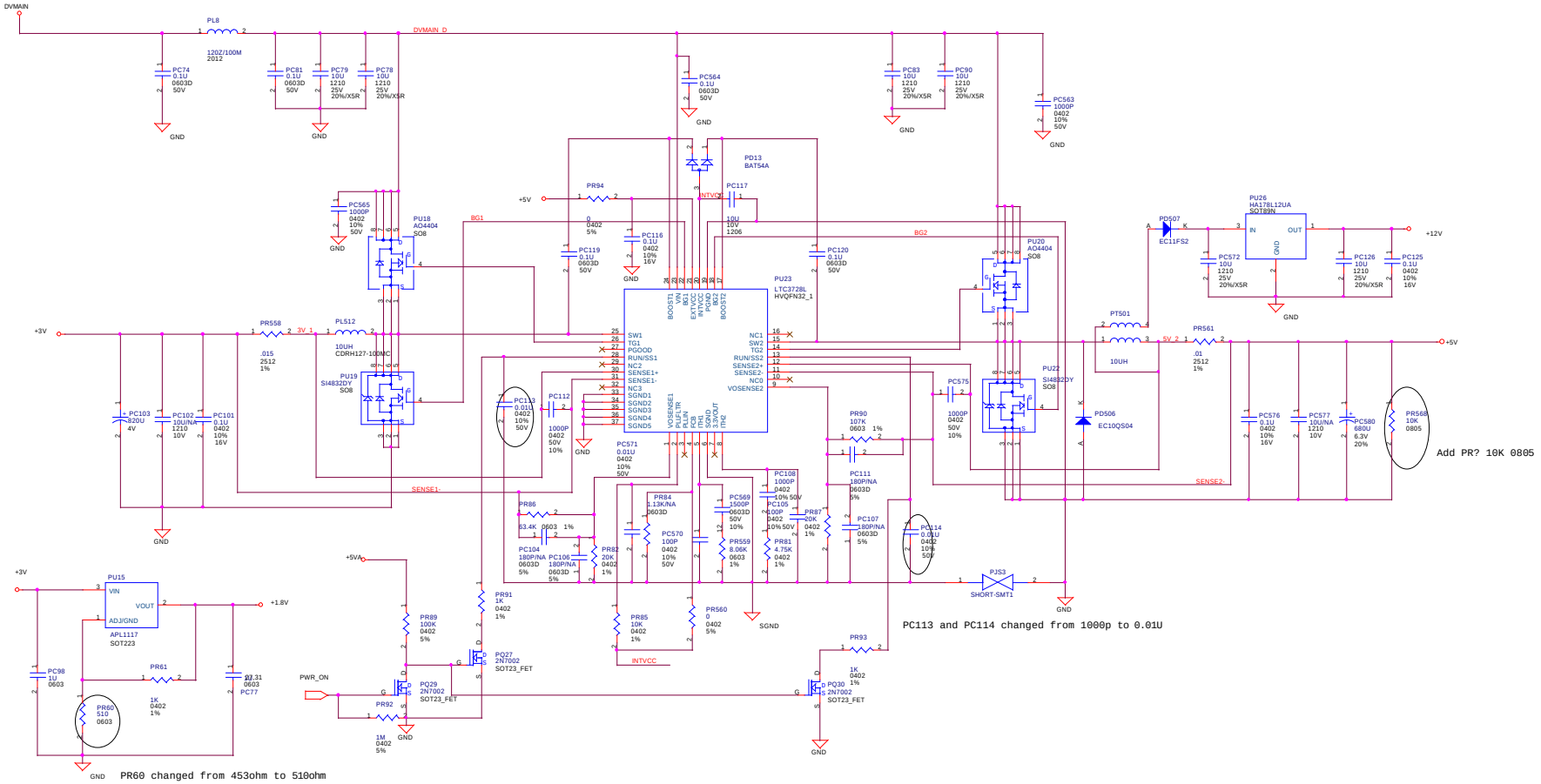

MiTAC

Title	+5V,+3V,+1.8V,+1.5V
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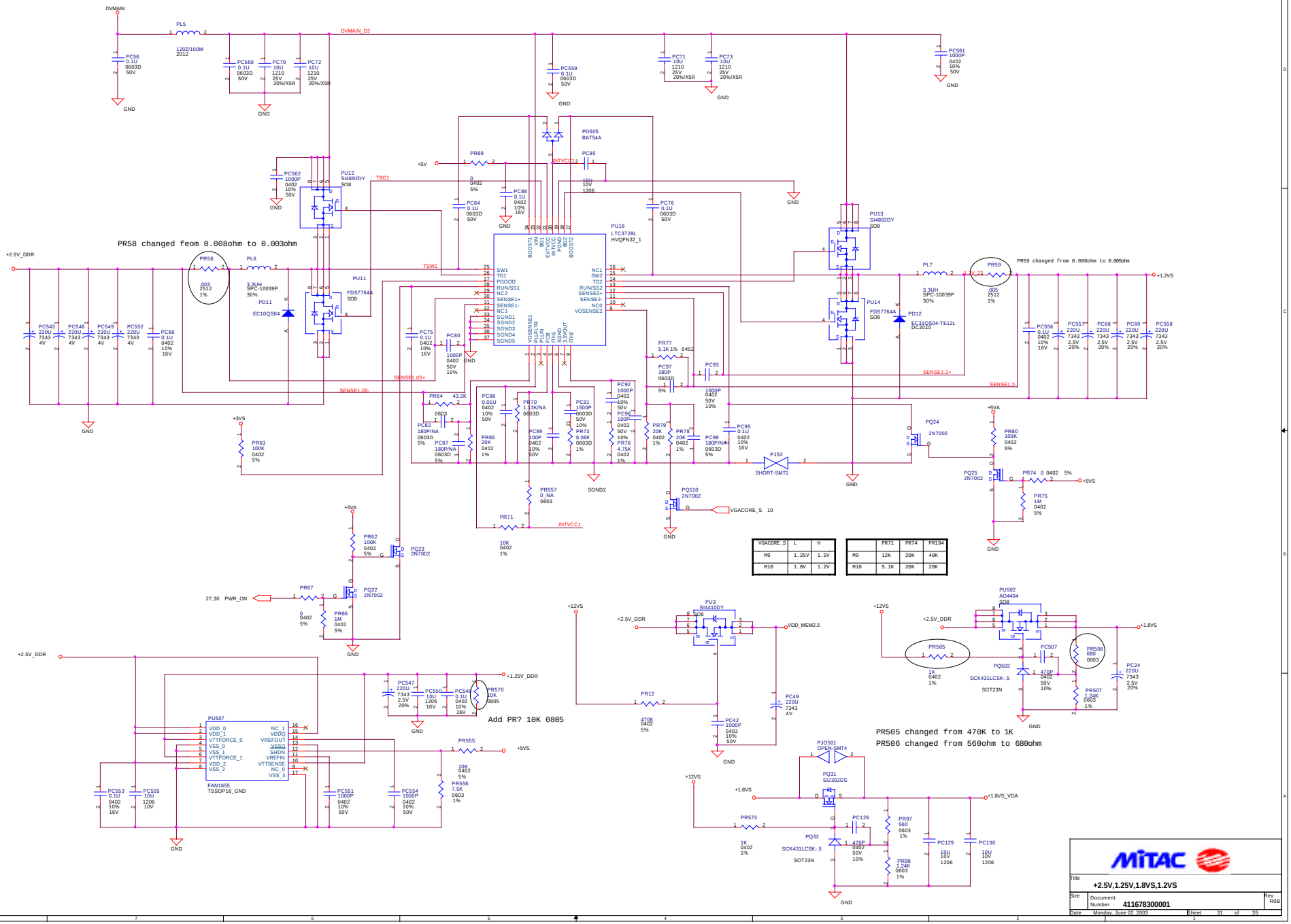
PR58 changed feom 0.008ohm to 0.003ohm
PR59 changed from 0.008ohm to 0.005ohm
Add PR? 10K 0805
PR505 changed from 470K to 1K
PR506 changed from 560ohm to 680ohm
VGACORE_S L H
M9 1.25V 1.5V
M10 1.0V 1.2V
PR71 PR74 PR194
M9 12K 20K 40K
M10 5.1K 20K 20K
Title +2.5V,1.25V,1.8VS,1.2VS
Number 411678300001
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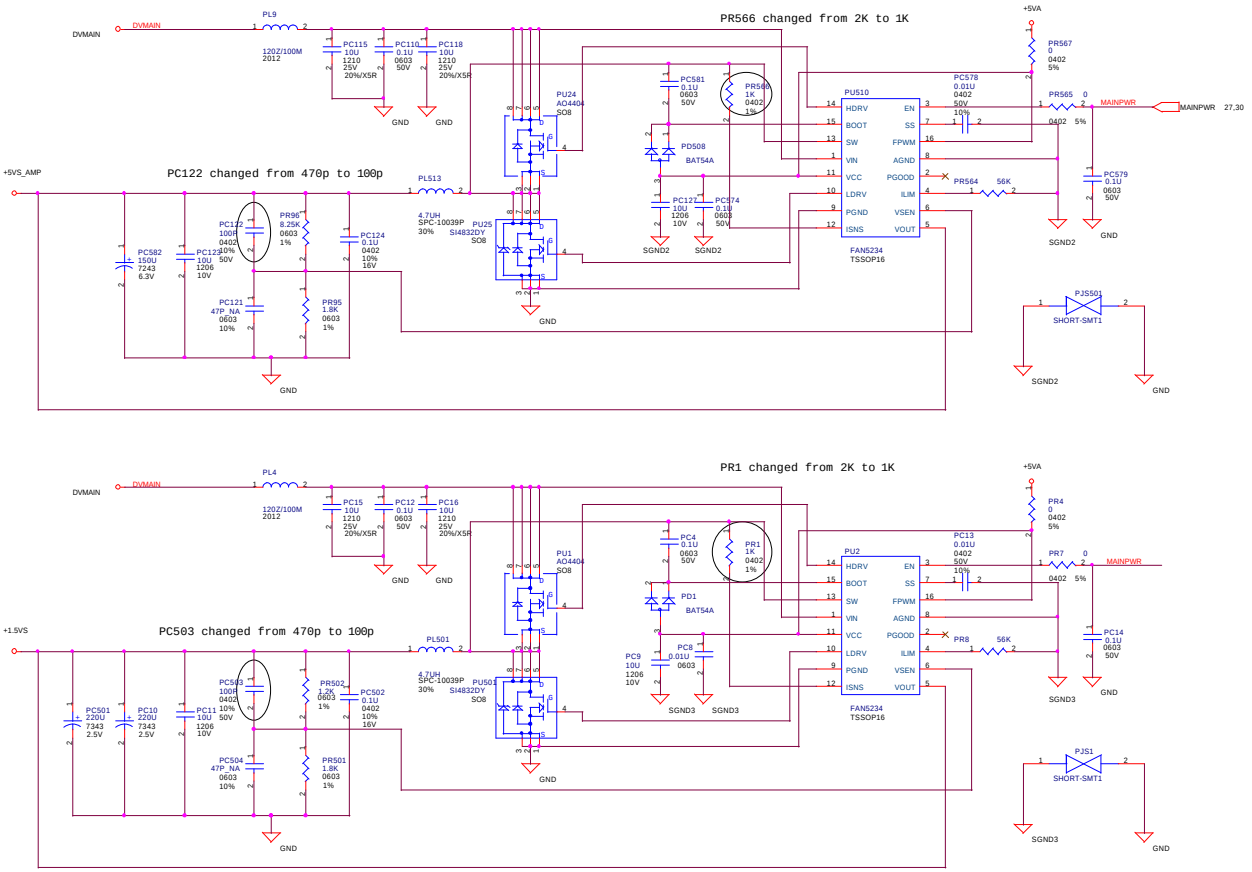

MiTAC		
Title	5V_AMP,+1.5VS	
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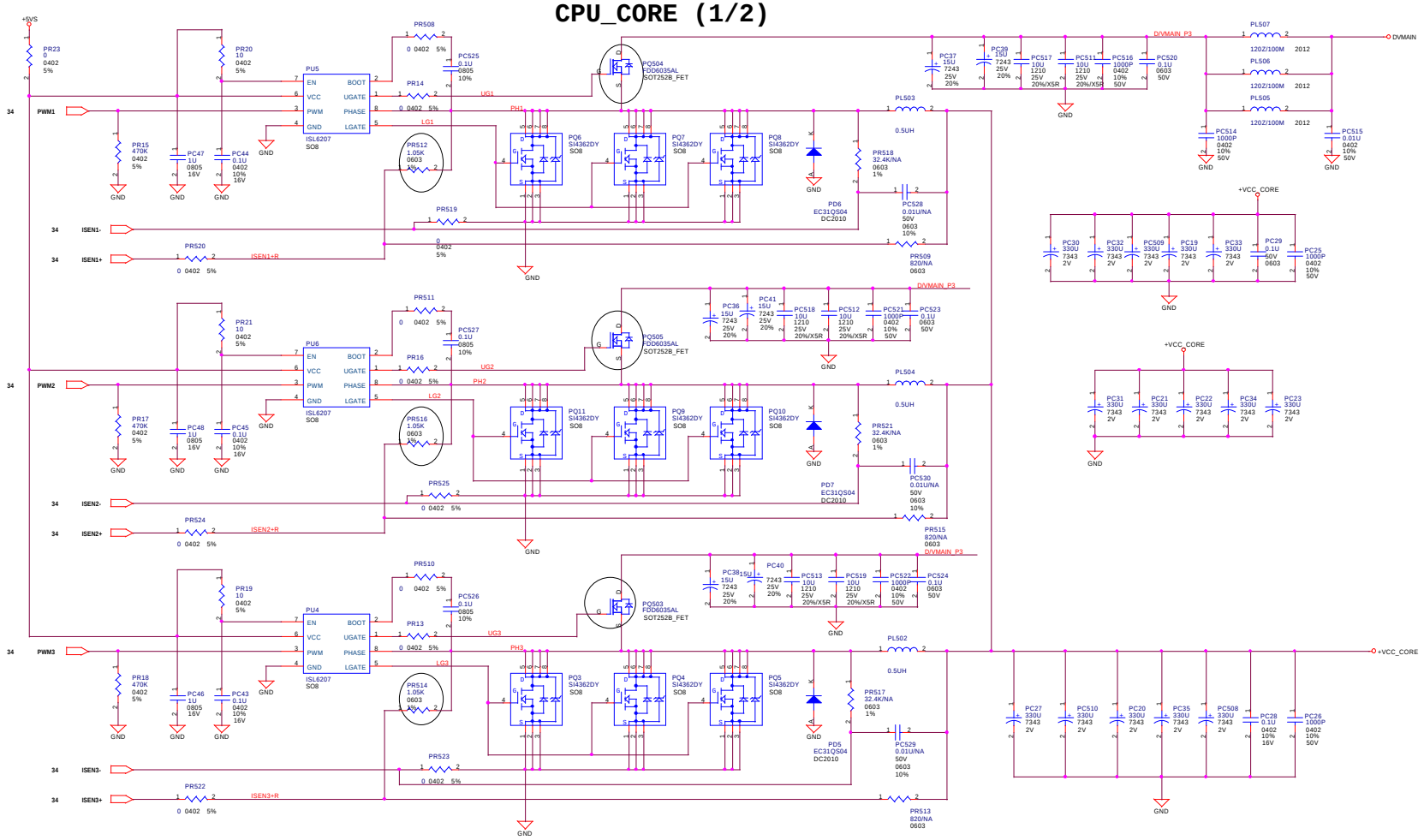
CPU_CORE (1/2)



PQ503,PQ504,PQ505 changed from FDD6612A to FDD6035AL
PR512,PR514,PR516 changed from 3.57K to 1.05K

Title	CPU_CORE1
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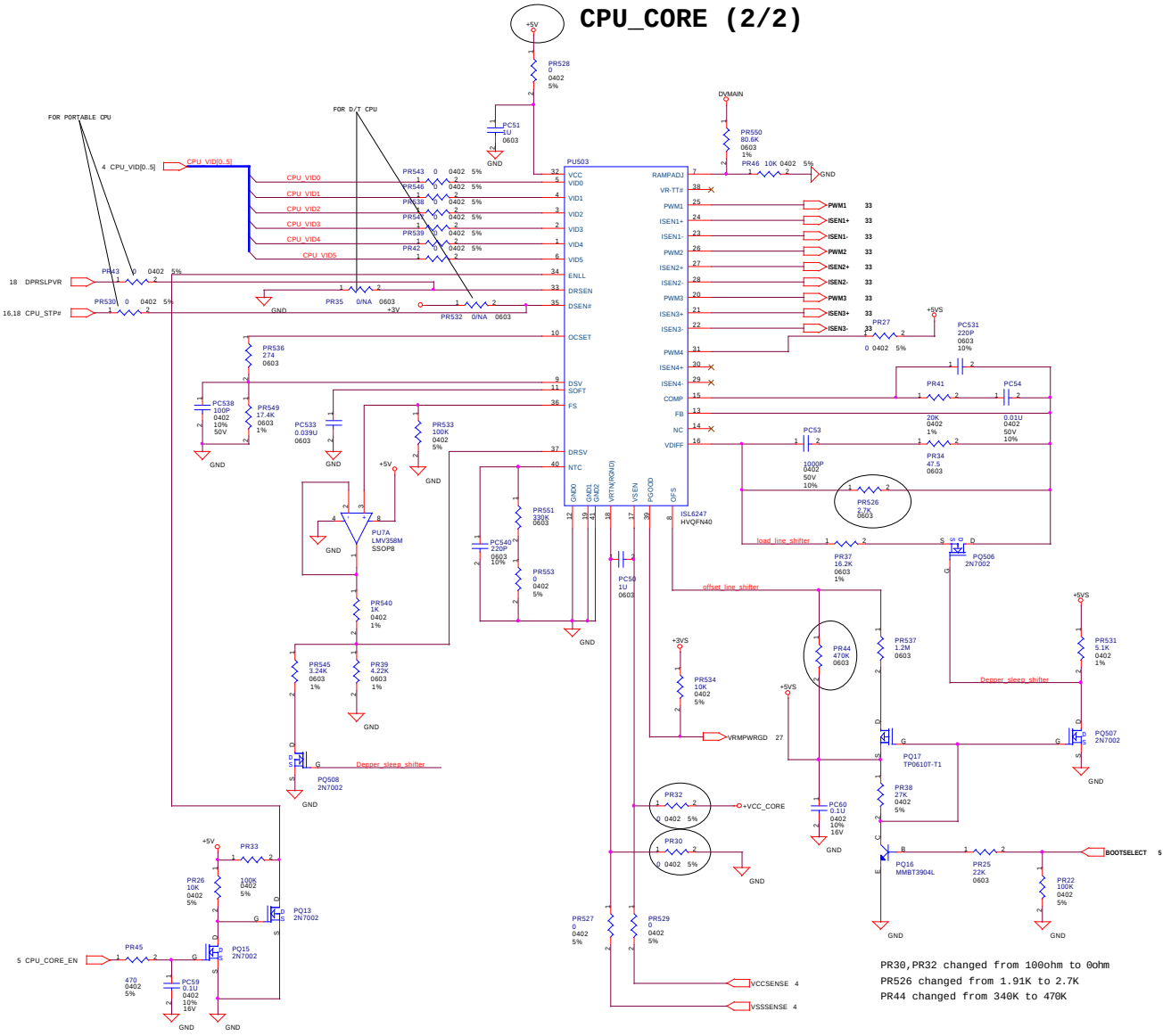
PR528 pin1 changed from +5VS to +5V

CPU_CORE (2/2)



PR30,PR32 changed from 100ohm to 0ohm
PR526 changed from 1.91K to 2.7K
PR44 changed from 340K to 470K

Title	CPU_CORE2	
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HISTORY

PAGE 4 ADD JUNCTION FOR R0A LOSE
PAGE 5 Change CAP. from 10uF to 22uF
PAGE 6 Delete RP5 for CRT detect
PAGE 10 Change R618 from 60.4 ohm to 0 ohm
PAGE 10 Add R132 from N/A to mount for S3 leakage
PAGE 11 Change L538,L539 from 120Z/100M to 0 ohm for voltage level issue
PAGE 12 Delete
RP526,RP536,RP528,RP529,RP544,RP545,RP22,RP32,RP539,RP540,RP537,RP538,RP541,RP542
,RP34,RP36,RP578,RP574,RP575,RP579,RP15,RP23,RP33,RP35,RP580,R629,C649,C648,C205,C200,C653
,C651,C655,C652,C659,C227,C675,C195,C676
PAGE 13 Delete
RP523,RP547,RP543,RP530,RP527,RP548,RP546,RP24,RP513,RP511,RP521,RP509,RP507,RP517,RP515,
RP28,RP26,RP38,RP37,RP40,RP13,RP11,RP17,C592,C619,C627,C646,C191,C647,C650,C201,C198,C197,C203,C210,C204
PAGE 14 Add R802,R803,R804,R805,C903,C904,C905,C906 in CKE signal for cover noise
PAGE 15 Add U528,U529 in HSYNC and VSYNC
PAGE 16 Change C256 and C257 from 10P to 12P for in XP timer.
PAGE 18 Change C313,C318 from 20P to 12P
PAGE 19 Change U15 from HP to Sharp
PAGE 20 Modify touch pad voltage from +5V to +5VS
PAGE 21 Add D510 in U523's REQ# for leakage voltage
PAGE 24 Add R807,R808 8.2K bewteen U14 to CAP for adjust big sound
PAGE 27 PWROK signal add level shift
PAGE 27 change KB_S and BATT_G# signal for BATT_G# have noise during boot

MiTAC

Title	HISTORY	
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Reference Material

- **Mobil Intel Pentium 4 Processor-M ……..…….. ……..…** ***Intel Corp***
- **SiS648FX Data Sheet ……*Silicon Integrated Systems Corp***
- **SiS963 Data Sheet ……*Silicon Integrated Systems Corp***
- **8555 Hardware Engineering Specification ……. *Technology Corp./MiTAC***

SERVICE MANUAL FOR 8555

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Publisher : MiTAC International Corp.

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First Edition : Oct. 2003

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